Symmetry Computation for Hierarchical Analog Designs

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Constraint-Driven Design

- state of the art: computation for flat netlists, e.g., [1,2,4,5]
- BUT: real designs use a design hierarchy

Method

Challenge: modelling of subcircuits in ESFG symmetry allowed or forbidden among generated edges

Comparison

Investigated circuit: instrumentation amplifier (see right)

<table>
<thead>
<tr>
<th>symmetry pairs</th>
<th>runtime</th>
</tr>
</thead>
<tbody>
<tr>
<td>(transistor level)</td>
<td></td>
</tr>
<tr>
<td>between I1 - I2</td>
<td>10</td>
</tr>
<tr>
<td>inside I3</td>
<td>3.8x</td>
</tr>
<tr>
<td>top level</td>
<td></td>
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</tbody>
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