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Generation of Piecewise-Linear Semiconductor Models for Accelerated Mixed-Signal Simulation

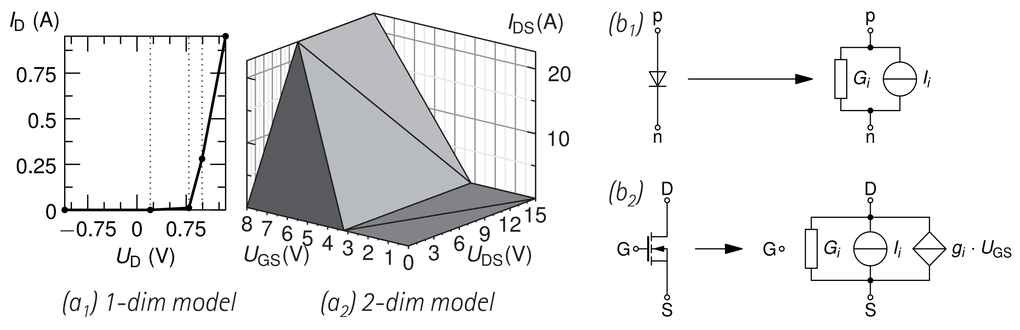
Abstract

The success of mixed-signal systems in recent years requires new design automation efforts in several areas. One important topic is to perform verification in an acceptable time.
We present efficient methods for piecewise-linear (PWL) model generation of semiconductor devices for accelerated mixed-signal simulation. The acceleration of our simulation approach is accomplished by not requiring any numerical integration. For this purpose, all nonlinear device models of an analog circuit have to be replaced with PWL models. The possible combinations of these PWL element models result in a set of circuit-model regions. Each circuit-model region corresponds to a linear state-space representation. The simulation kernel automatically switches between valid regions of these PWL models when computing the simulation results. The acceleration is achieved by efficiently evaluating equations of the following

$$\boldsymbol{x}(t) = e^{\boldsymbol{A}t}\left(\boldsymbol{x}_0 + \boldsymbol{A}^{-1}\boldsymbol{B}\boldsymbol{u}(t)\right) - \boldsymbol{A}^{-1}\boldsymbol{B}\boldsymbol{u}(t)$$
$$\boldsymbol{y}(t) = \boldsymbol{C}\boldsymbol{x}(t) + \boldsymbol{D}\boldsymbol{u}(t)$$

Diode Modeling (1-dimensional PWL Model)

Based on the Shockley equation, the characteristic curve $I_D(U_D)$ is discretized with a large number of initial data points. Interconnections between data points are called polylines. For the reduction of polylines we use dynamic programming to compute a global optimum approximation with a given number of segments.



(a_1) 1-dim model (a_2) 2-dim model

Exemplary 1-dimensional (a_1) and 2-dimensional (a_2) piecewise-linear models of semiconductor devices. The corresponding piecewise-linear equivalent circuits are shown in (b_1) and (b_2).

Characteristics

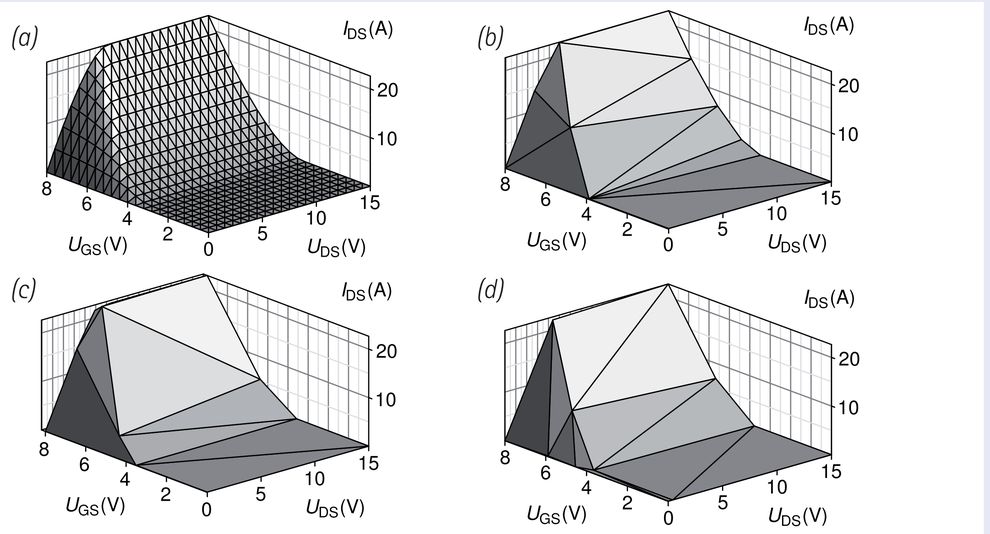
- Transient analysis of analog/mixed-signal circuits
- Event-driven simulation only depends on input changes
- Replacing nonlinear elements with piecewise-linear models
- Generation of PWL models by using geometric methods
- Determining initial grid by simulation of compact models or even by measuring real devices

Transistor Modeling (2-dimensional PWL Model)

The set of characteristic curves is modeled as a triangulated surface. For the reduction of triangles we have investigated three different simplification techniques. The first algorithm by Lindstrom and Turk is called "Memoryless Simplification" and the second by Garland and Heckbert is called "Quadric Error Metrics". Both algorithms do not guarantee that the outer boundary of the reduced surface still has its rectangular form. The newly developed method based on Simulated Annealing (SA) preserves the characteristic structure of a given initial surface while providing good results. It optimizes the triangulation by randomly moving vertices and accepting new triangulations based on the cost function

$$C = \sum_{i_1}^{N1}\sum_{i_2}^{N2} d_{i_1 i_2}^2$$

where $d_{i_1 i_2}$ is the distance in I_{DS}-axis direction between a data point of the initial grid and the intersection with the covering triangle. The resolution of the initial grid can be defined by the user. Although the SA algorithm does not show the best costs, it reliably preserves the outer boundary of the initial surface.



Initial MOSFET triangulation using a 20×20 grid (a) and MOSFET surface simplification results generated by "Memoryless Simplification" (b), "Quadric Error Metrics" (c) and Simulated Annealing (d).

Type of Modeling	Total Cost
"Memoryless Simplification"	18.54
"Quadric Error Metrics"	34.96
Simulated Annealing	19.71

Modeling error for all three presented algorithms.

Combining one- and two-dimensional PWL models enables modeling of bipolar junction transistors or even hierarchical structures like inverters and Darlington transistors.

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