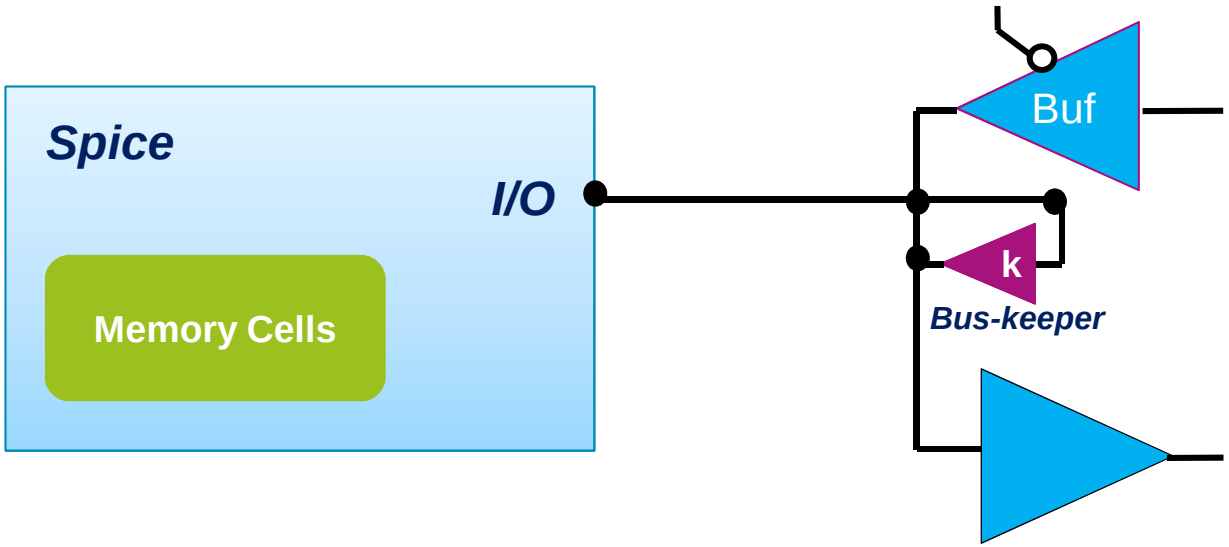
Strength-Based Analog/Digital Interface For AMS Simulation

Junwei Hou
Architect, Custom IC and Simulation
Cadence Design Systems

FAC 2013

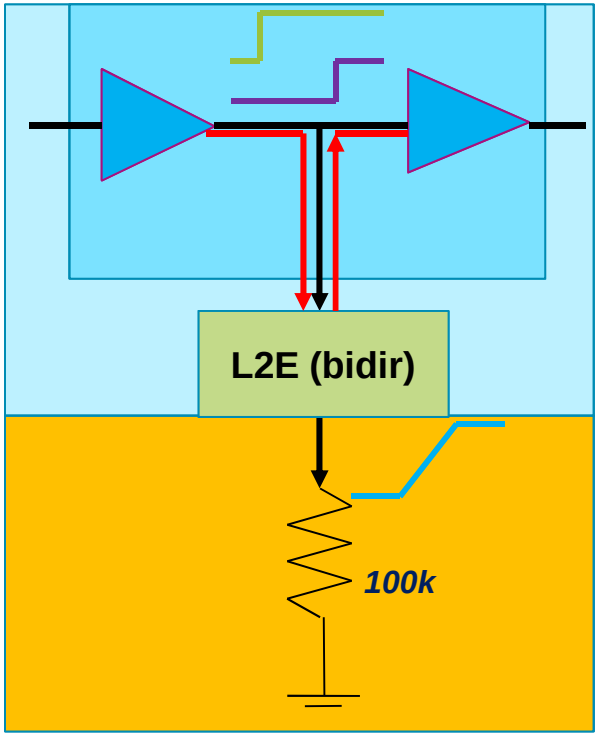
Functional-Level Mixed-Signal Verification Challenges

- Design with strength-based models in Verilog
  - Tran-gate, tri-state buffer, drivers with various strength levels
- Strength effect of Spice driver on mixed-signal net
  - A strong Spice driver can override a weak Verilog driver
- Dynamic bidirectional signals on mixed-signal net
  - Due to switching devices like tran-gate, tri-state buffer, etc.
- Apps: Bus-keeper, USB interface, Testbench bidir pin

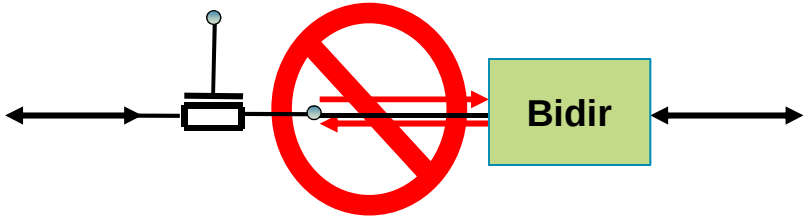


Chip-Level Mixed-Signal Verification Challenges

- Inaccuracy Due To Driver-Receiver Segregation (DRS)



•Over calculation of analog loading effect, causing timing (SDF) error



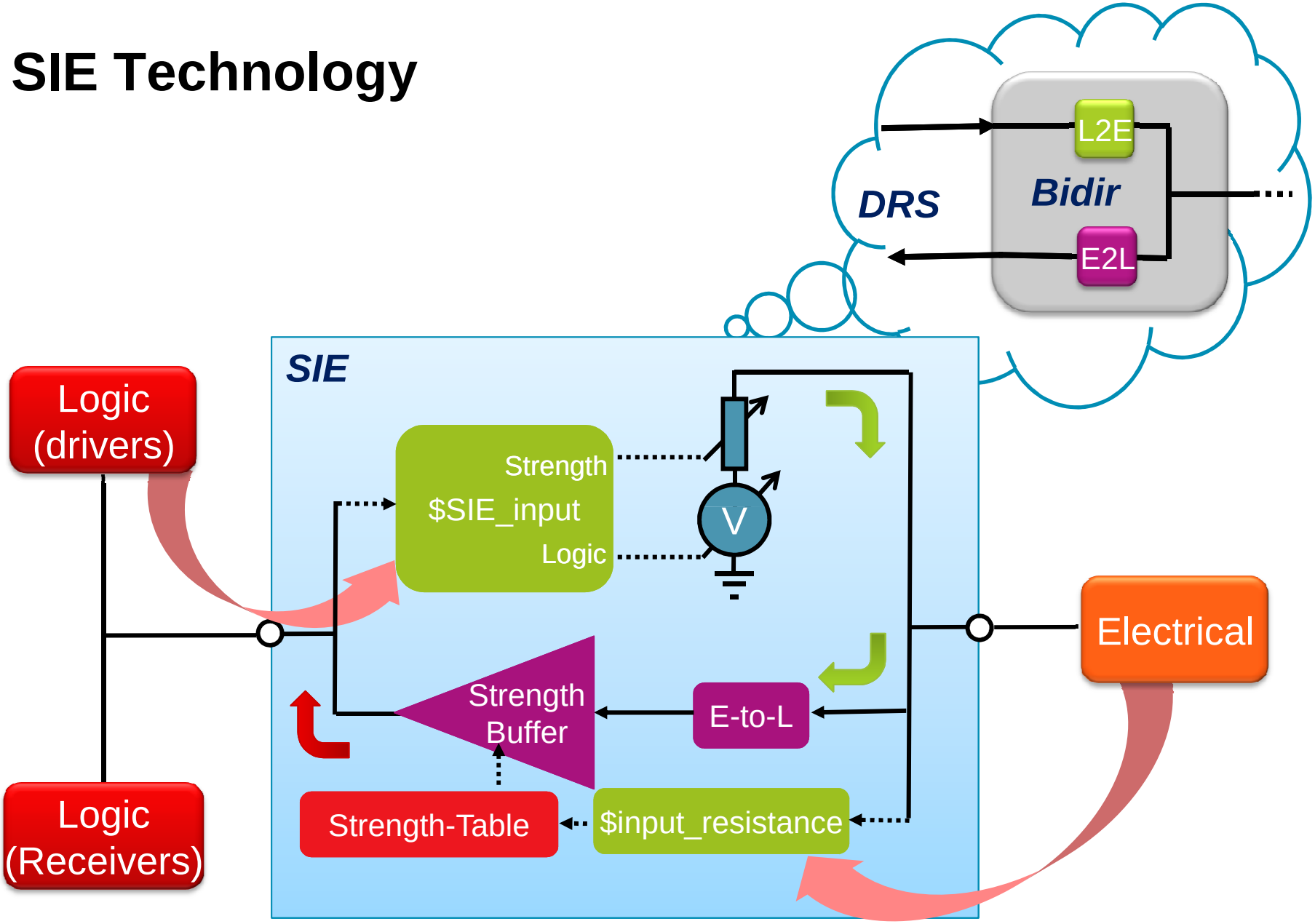
- Incorrect handling of tran-gate at mixed-signal connection

- Wrong value in IE probe

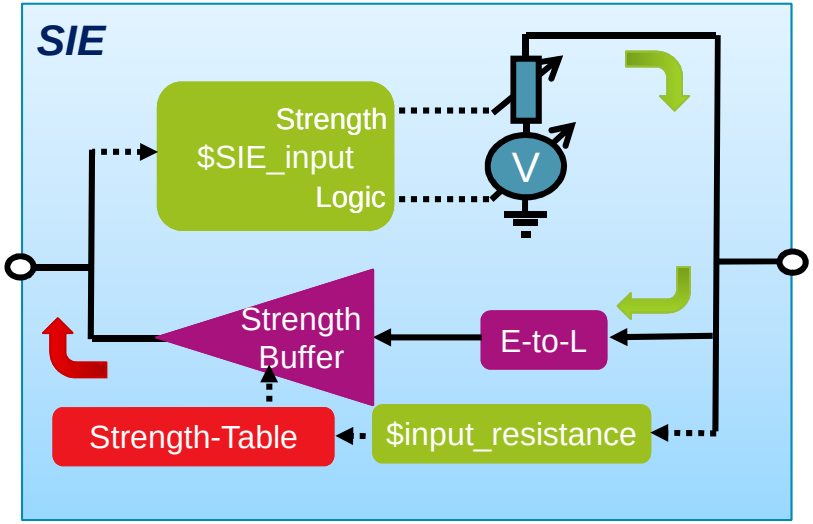
Solution: Strength-Based Interface Without DRS

- Strength-Based Interface Element (SIE) is inserted without DRS in mixed-signal net connecting analog and digital signals
- Conversion between logic value and strength of digital signal and voltage and resistance of analog Thevenin equivalent circuit
  - Instead of only voltage and logic value conversion of IE in DRS
- Analog accuracy in analog/digital signal conversion using Thevenin equivalent circuit
- The signal value and direction on the mixed-signal net are resolved automatically and dynamically

SIE Technology



SIE Technology

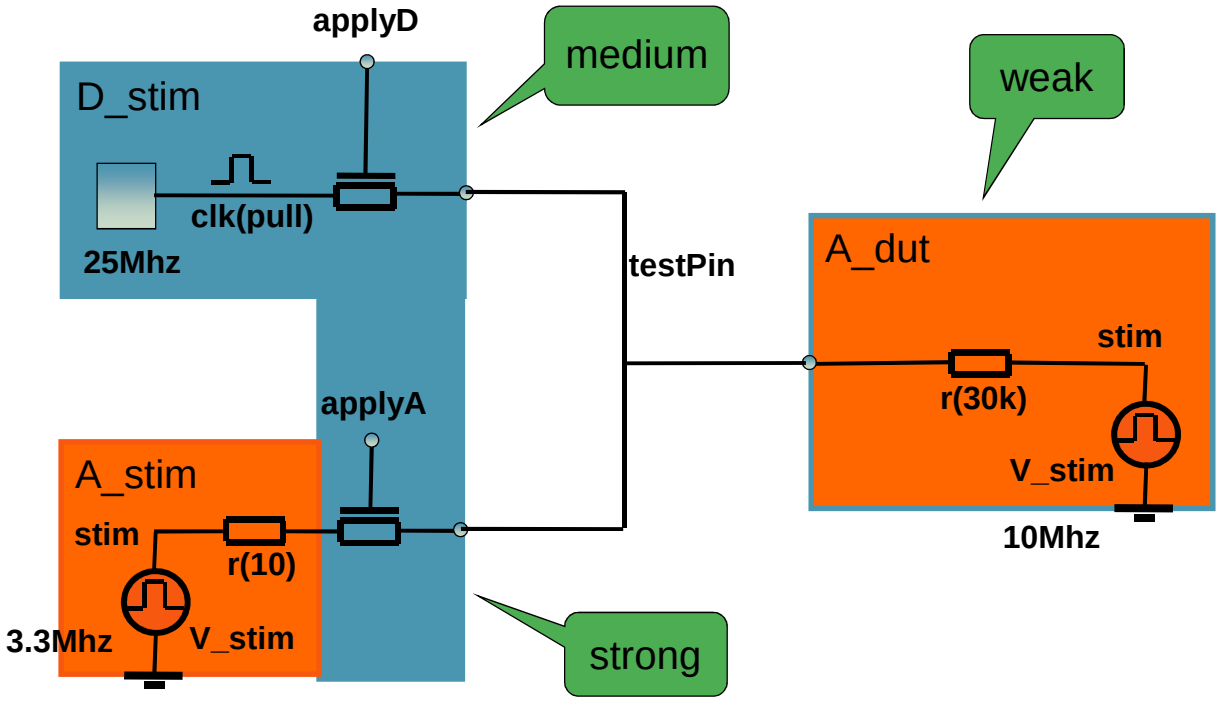


The port output resistance and the driving signal strength at that port are usually defined by the user

Strength	Level	Resistance
supply	7	1
strong	6	1e1
pull	5	1e2
large	4	1e3
weak	3	1e4
medium	2	1e5
small	1	1e6
highz	0	1e7

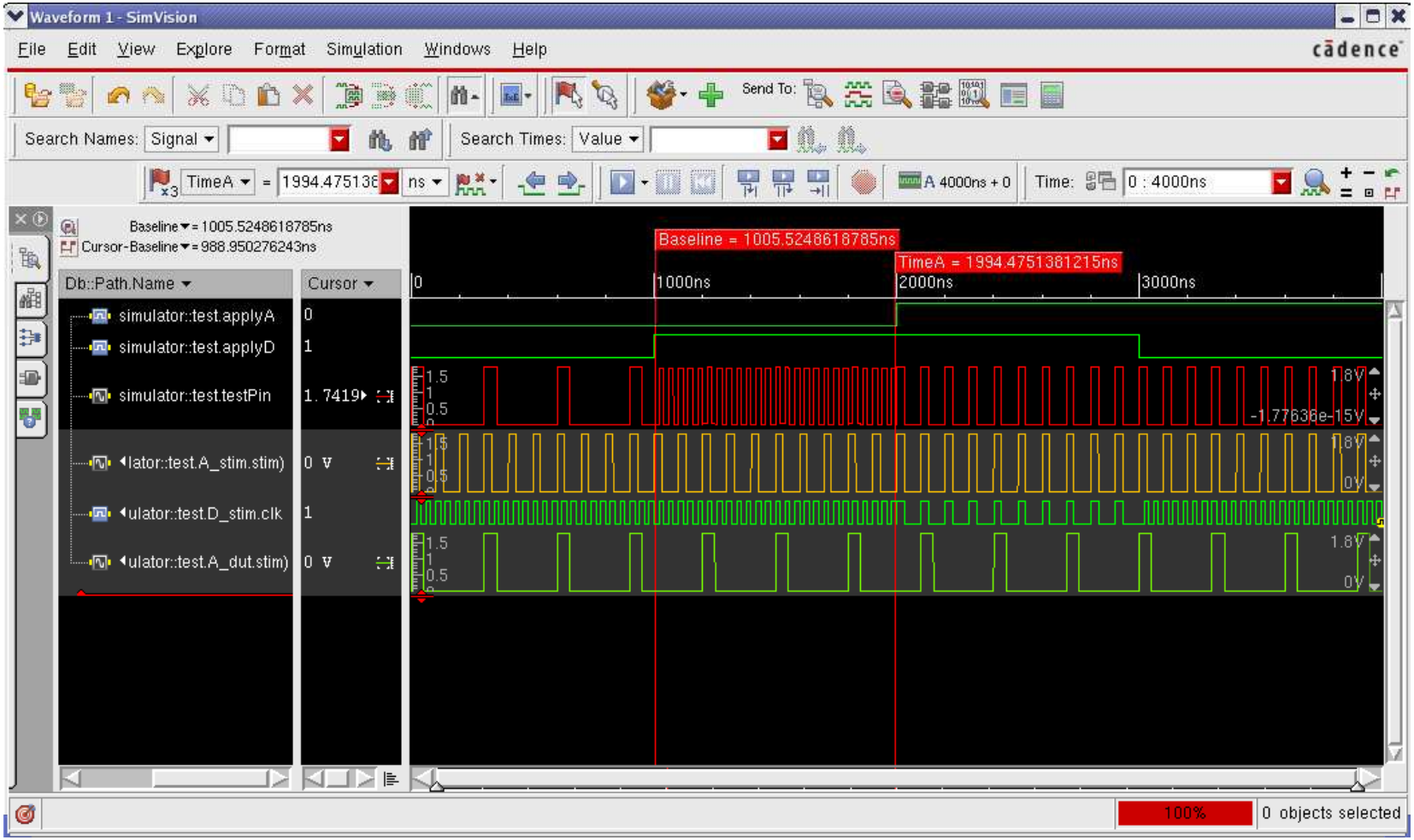
Tutorial Case

- D_stim is digital stimulus block in Verilog with tran-gate of medium strength
- A_stim is analog gated low-impedence stimulus block in Verilog-AMS
- A_dut is analog DUT of weak load in Verilog-AMS



Tutorial Case Simulation Results

- Simulation Results Using SIE Option Of AMS-Designer in IUS9.2 or Later;
- DRS IE gives wrong results



Application-1: Bidir Tran-Gate Connection

- Digital Block tran-gates connected to mixed-signal net
- As well as tri-gates, and/or any other types of digital devices on the mixed-signal net
- In any design hierarchy
- No need to declare port direction for modules in digital Block
- The simulator automatically resolves the signal direction

Application-2: Bidirectional Mixed-Signal Bus

- The signal direction on mixed-signal bus may change dynamically
  - When tran-gate/tri-gate in Digital Block turns ON/OFF
- Stronger Verilog signal may override mixed-signal net voltage level of Spice circuit
  - Spice circuits read/write Verilog memory cells, or vise versa
  - Analog Accuracy on mixed-signal bus
  - High-Z state of Spice circuit can be converted correctly to Verilog

Application-3: Bus Keeper On Mixed-Signal Bus

- Bus Keeper: A weaker driver with both input and output on the bus
- Keep the bus signal when other tran-gate/tri-gate drivers are OFF
- Bus keeper can be in either Spice or Verilog
- No need to workaround figuring out artificial output resistance in DRS Bidir.

Conclusions

1. Strength-Based IE Without DRS
   - Consistent with digital strength-based resolution algorithm for multiple drivers and hence more naturally fits into the digital technology;
   - Consistent with VHDL/VHDL-AMS connection which does not have the concept of DRS;
2. The Technology Also Enabled Wreal-Logic IE Without DRS
3. Accurately Support Strength-Based Applications With Vertually No Performance Overhead
   - **Bus-keeper, USB interface, Testbench with bidir pin, etc.**
4. Worry-free Simulation Configuration Of Various Verilog Models
5. Speed Up Simulation By Modeling Current-sensitive Devices In Verilog Tran Gates And Strength-based Models.

Thanks!