Statistical Verification of Analog Circuits

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- Behavioral verification 😊
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- Behavioral verification 😊
    - A lot of exciting progress
- Transistor-level 😟
    - Over-simplified device models
    - Unverified higher-level abstraction, e.g., op-amp models

About This Talk

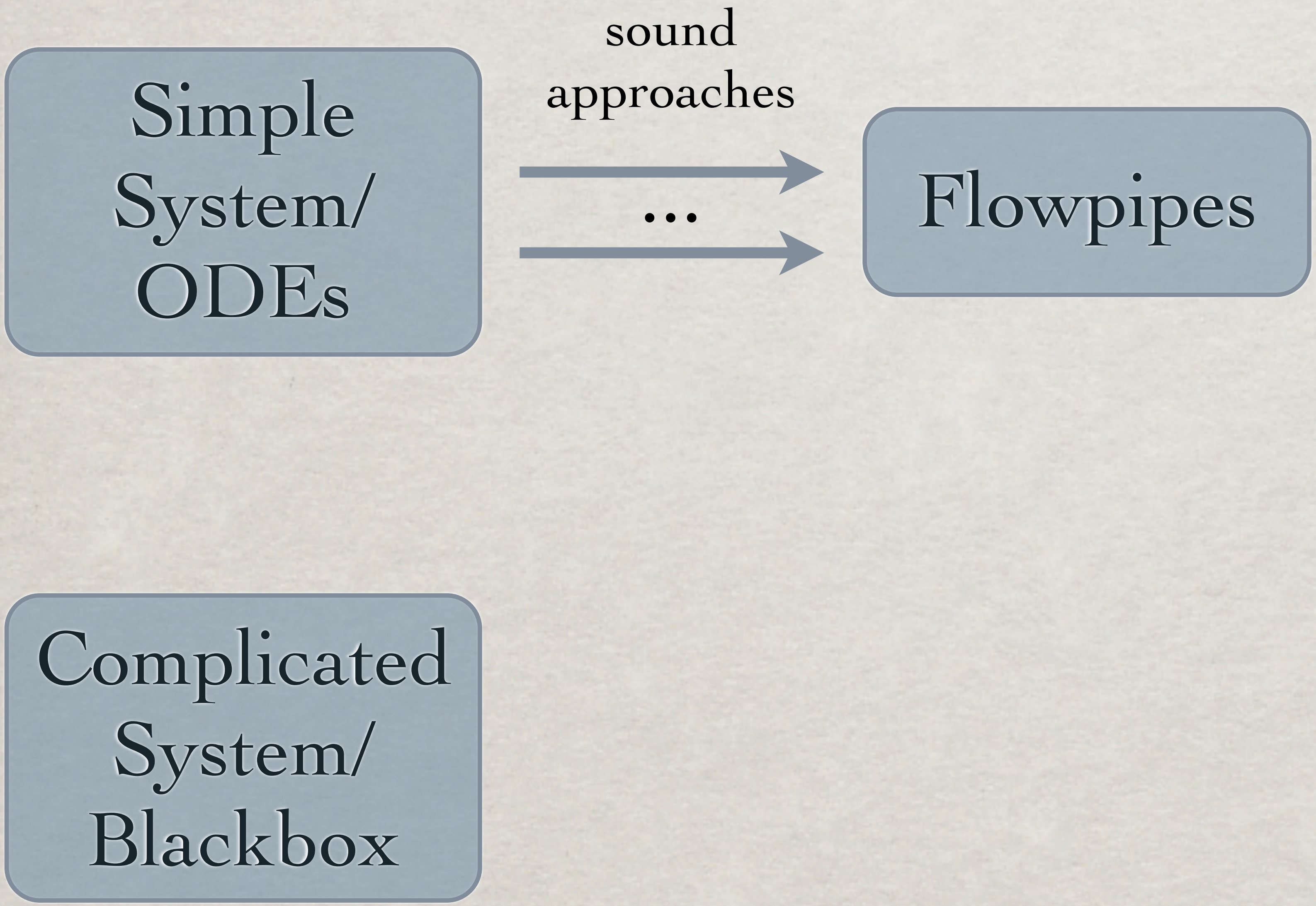
- Focus on transistor-level circuits
  - Variations: process, voltage, temperature
- Introduce a statistical verification approach
  - Verify interesting properties
  - Provide useful information to designers

Analog Circuits Are Hybrid Systems

Simple System/ ODEs

Complicated System/ Blackbox

Analog Circuits Are Hybrid Systems



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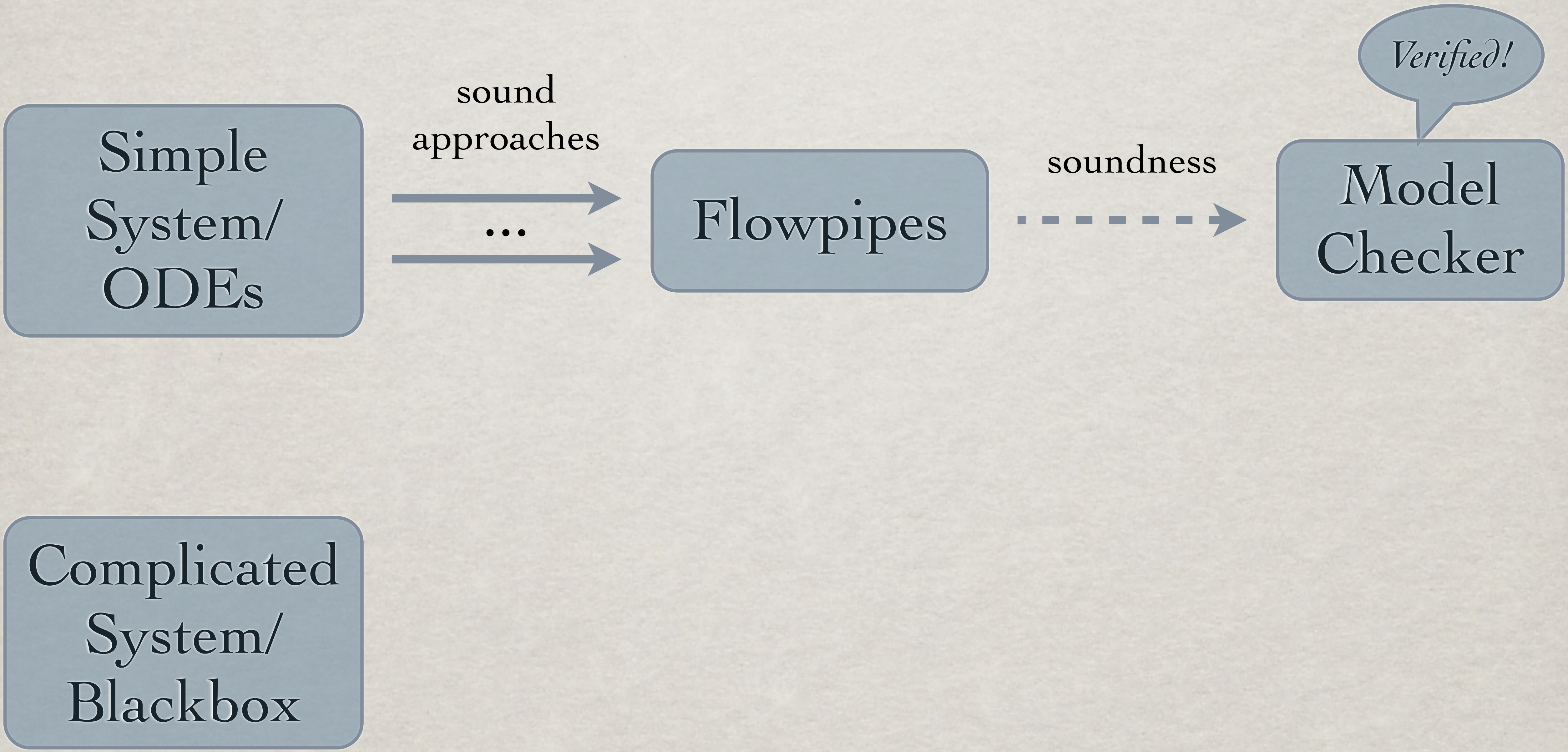

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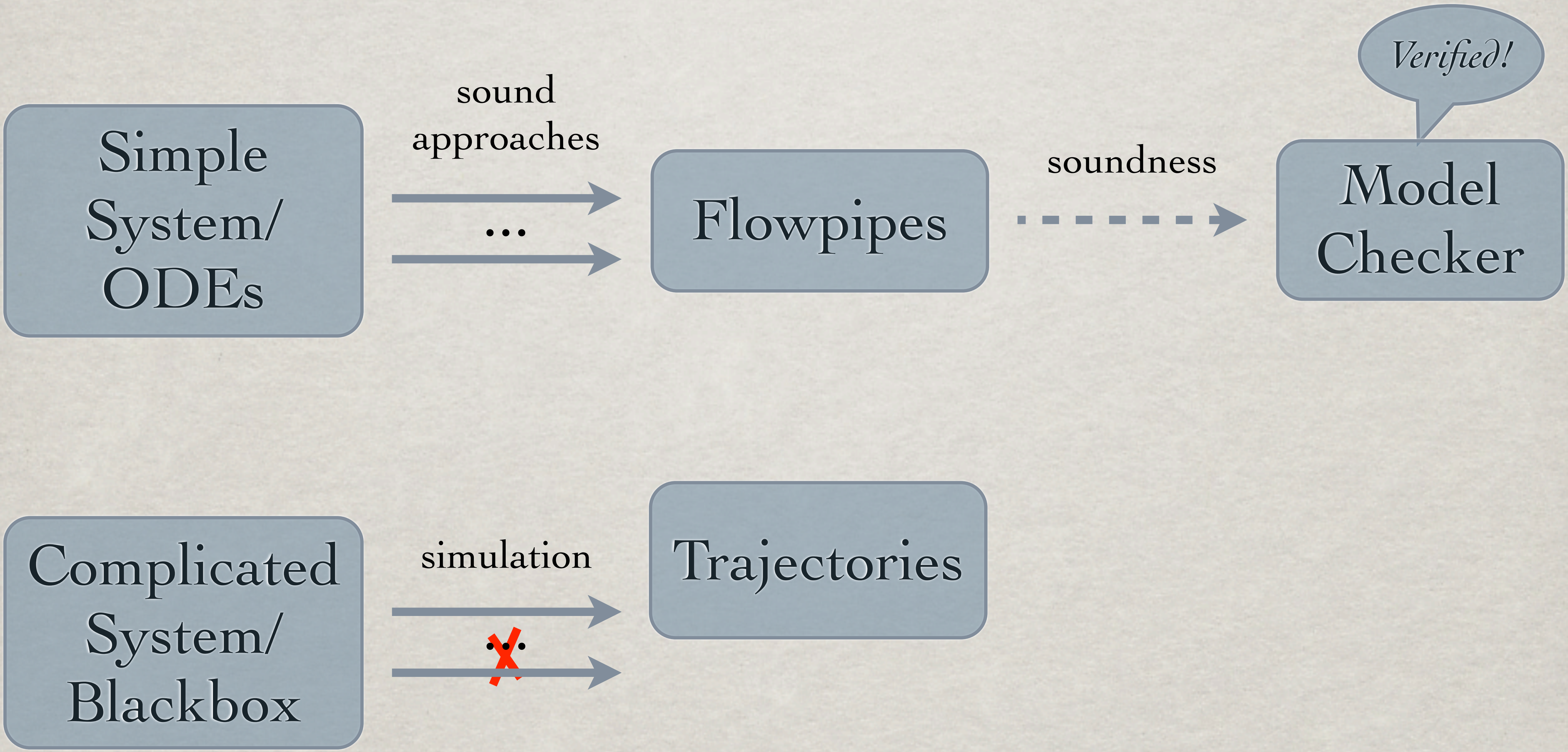

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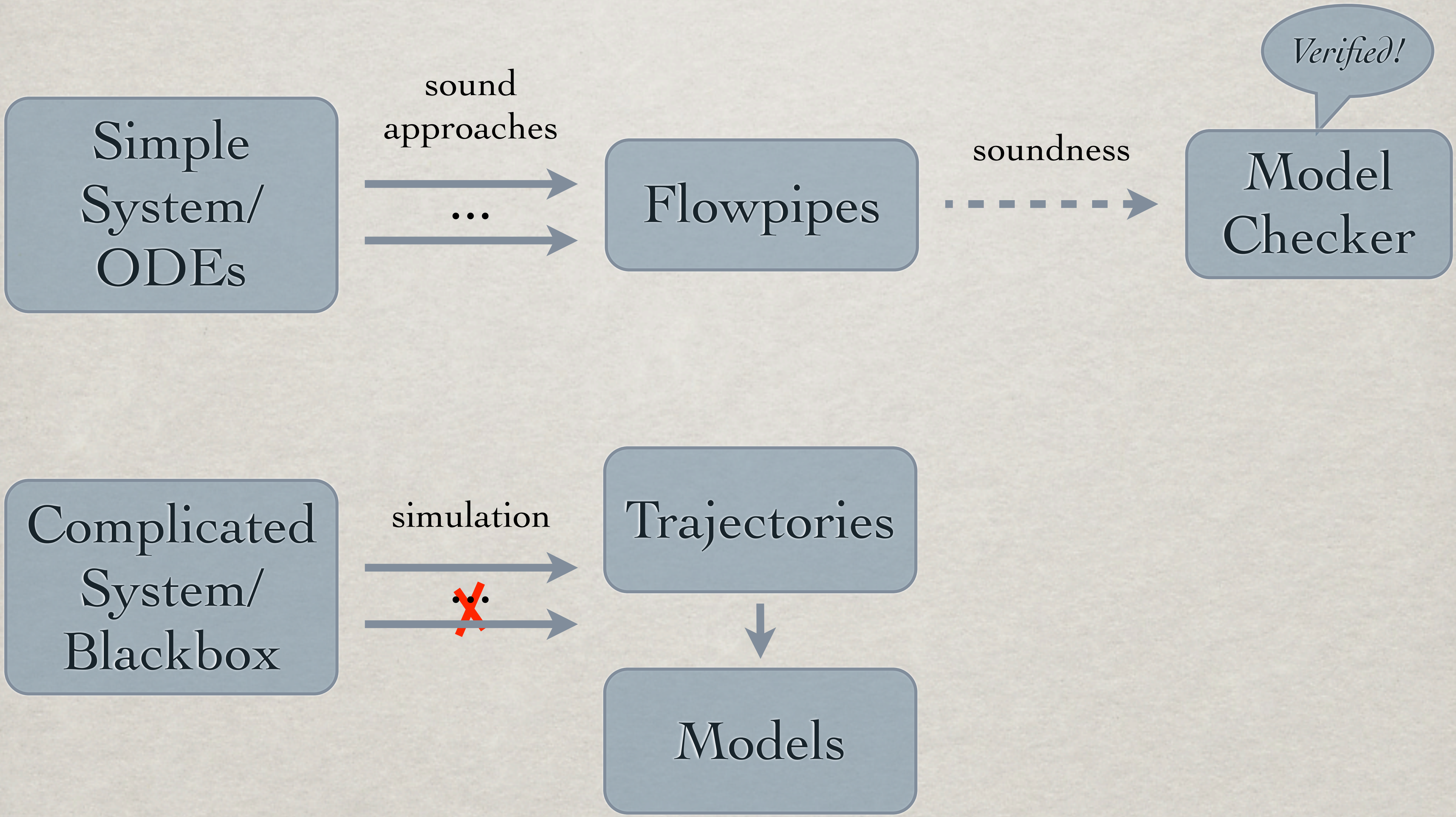

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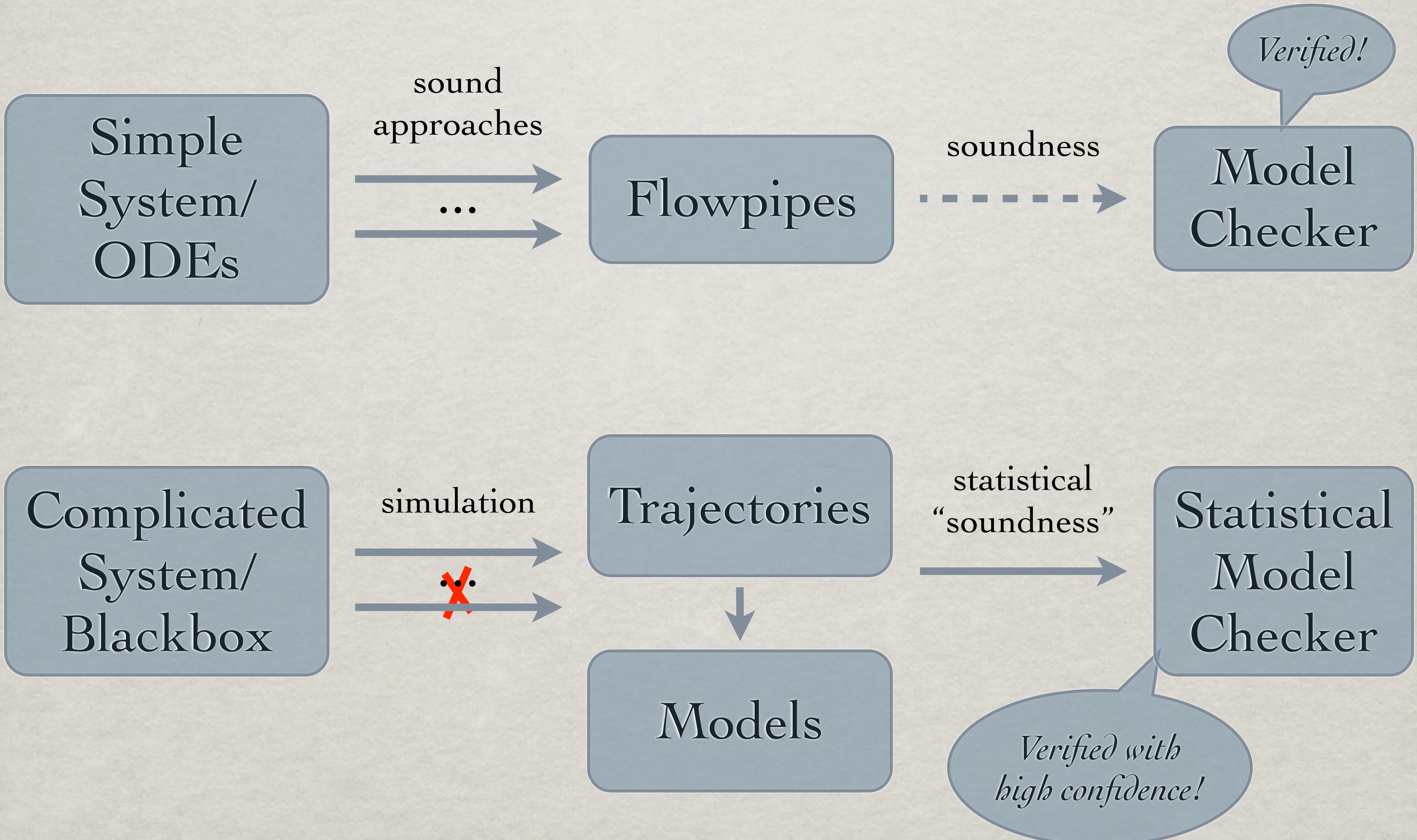

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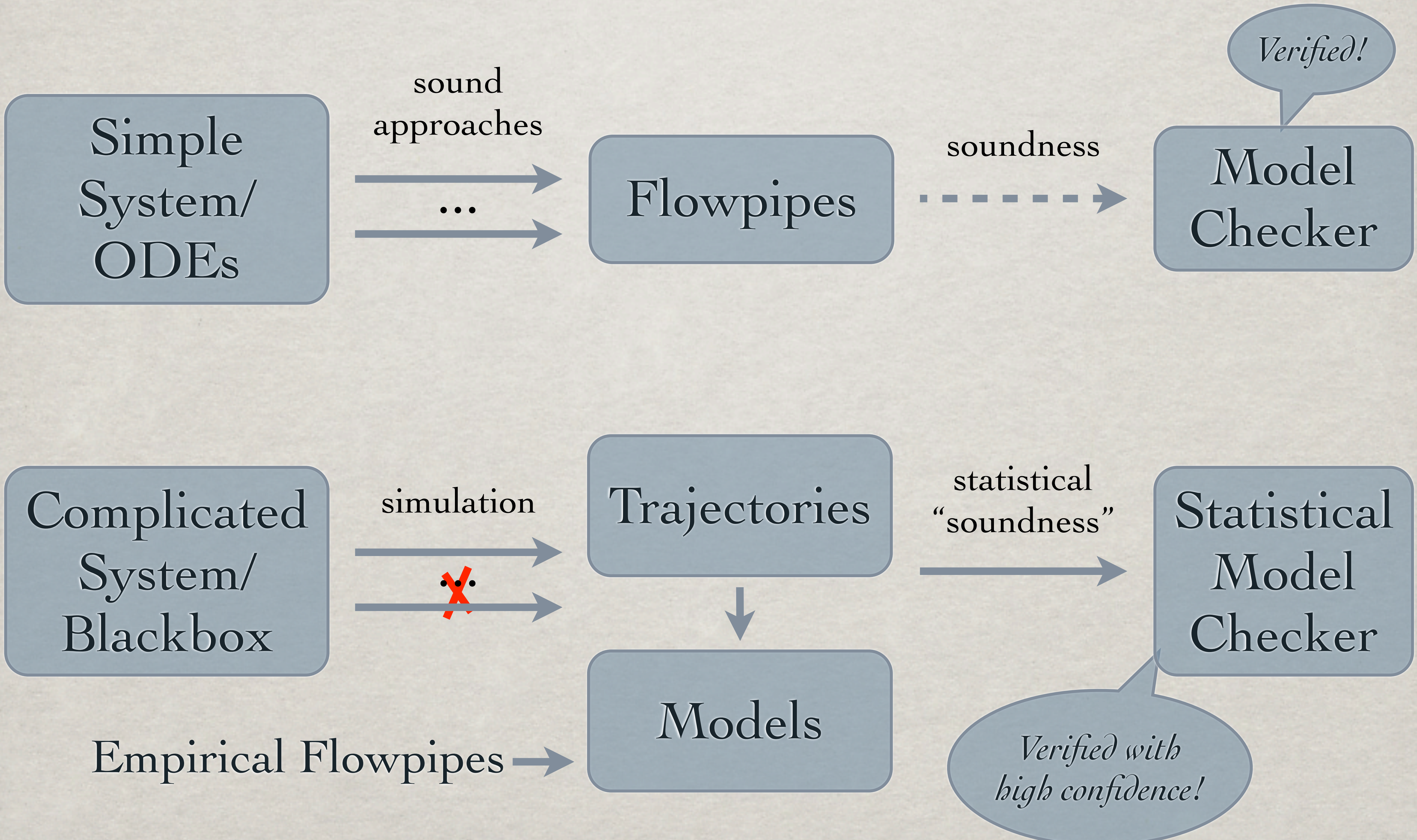
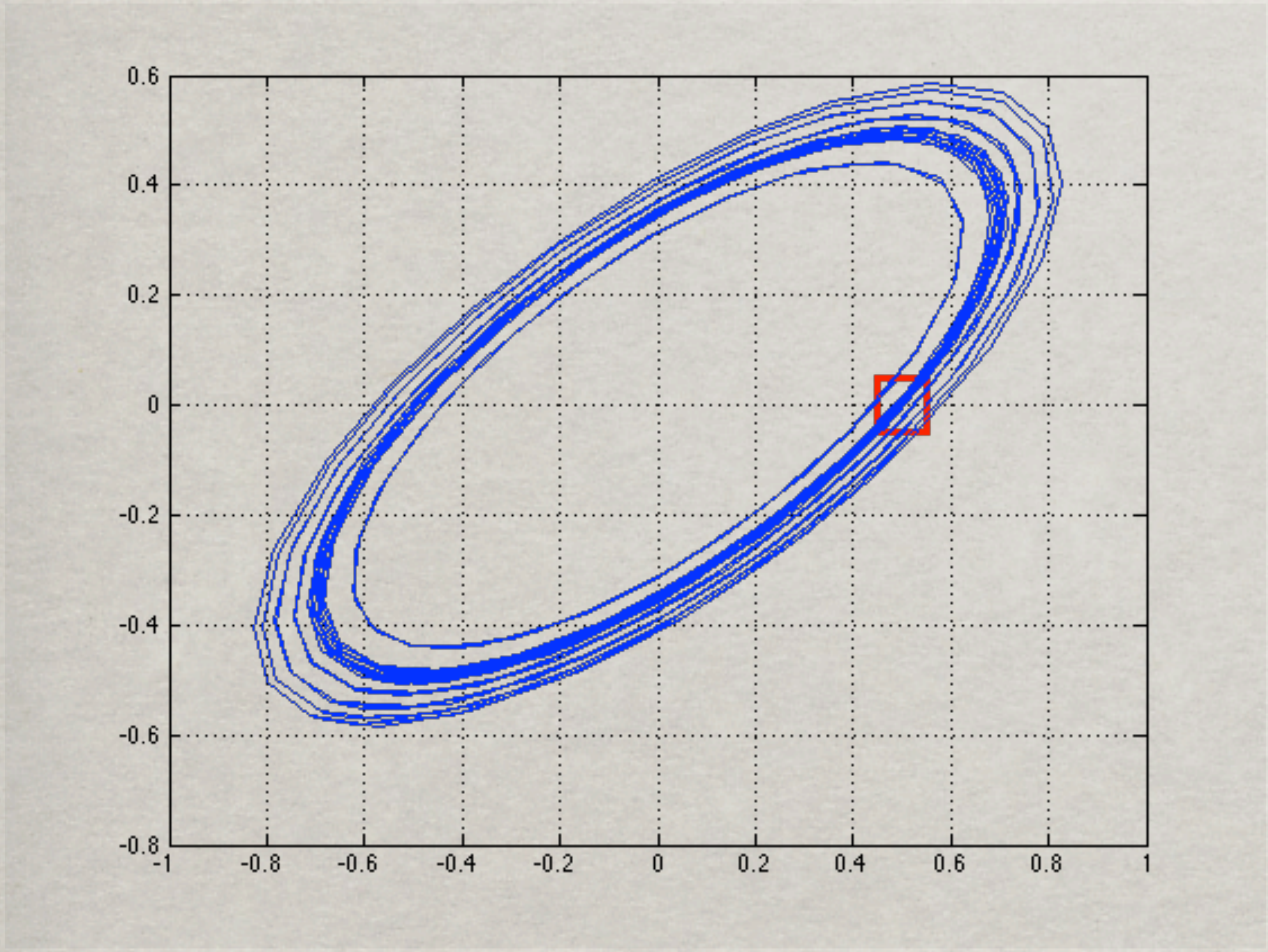


Learning Flowpipes



Unknown flow map F(x,t)

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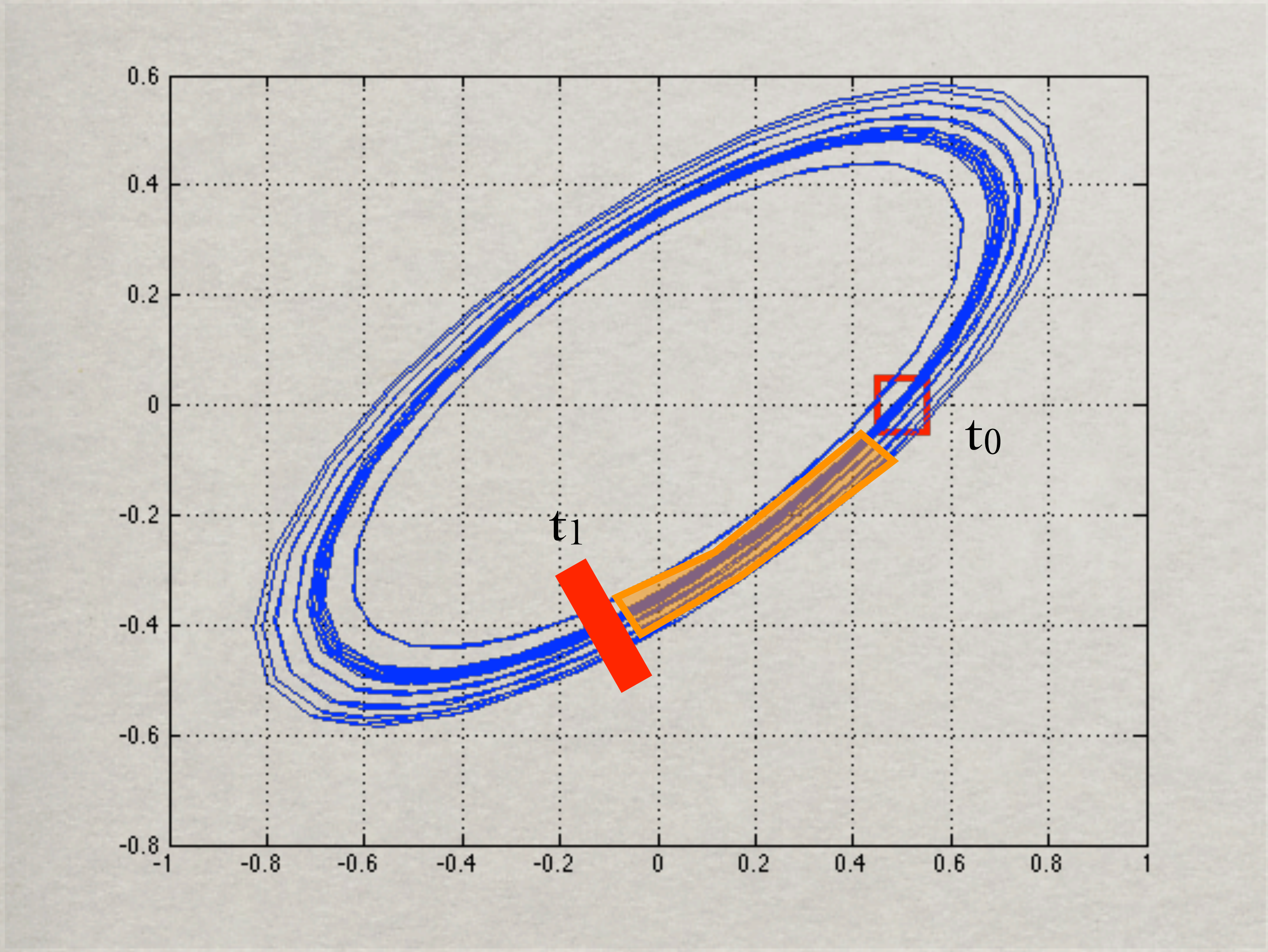

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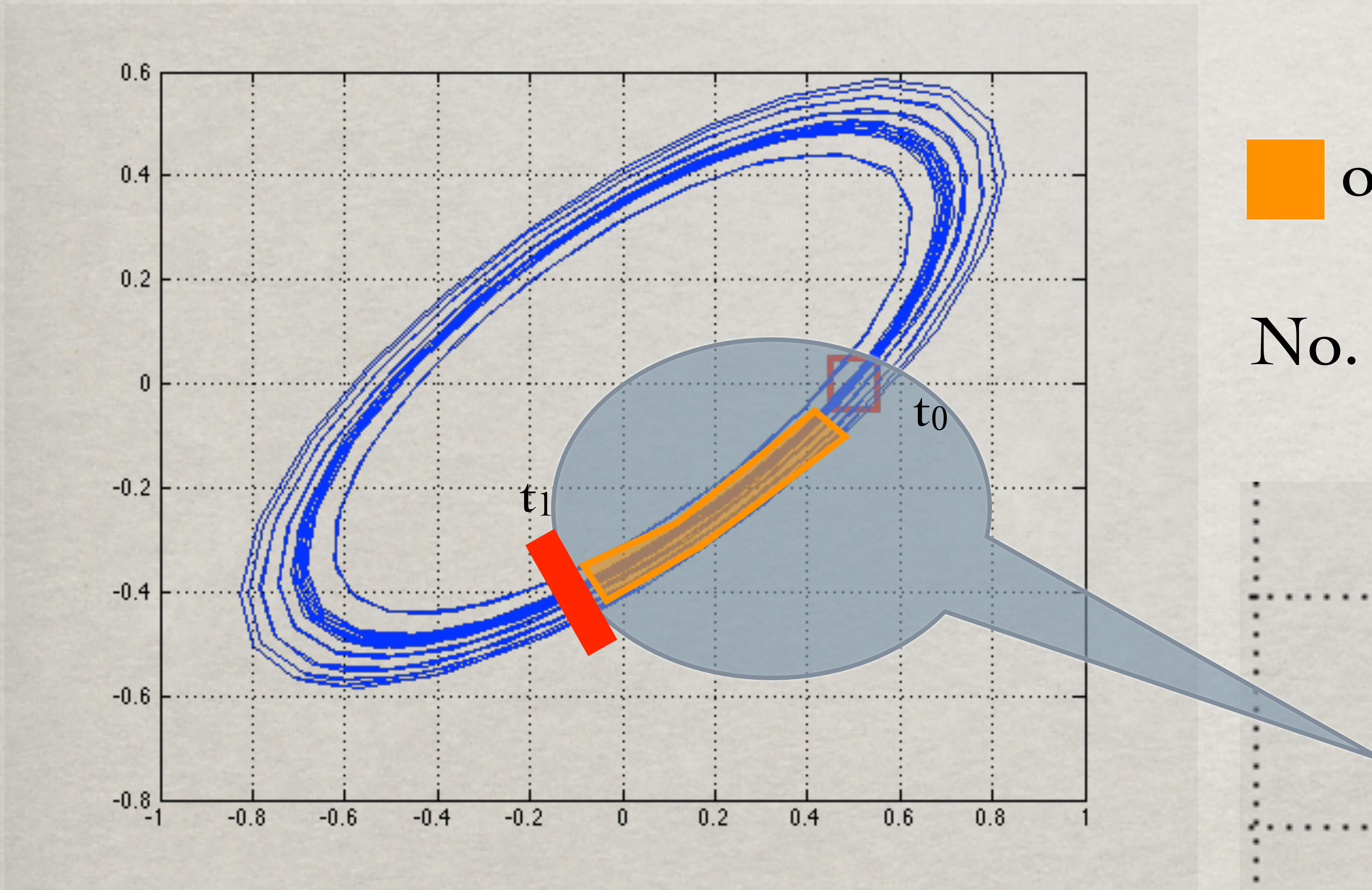

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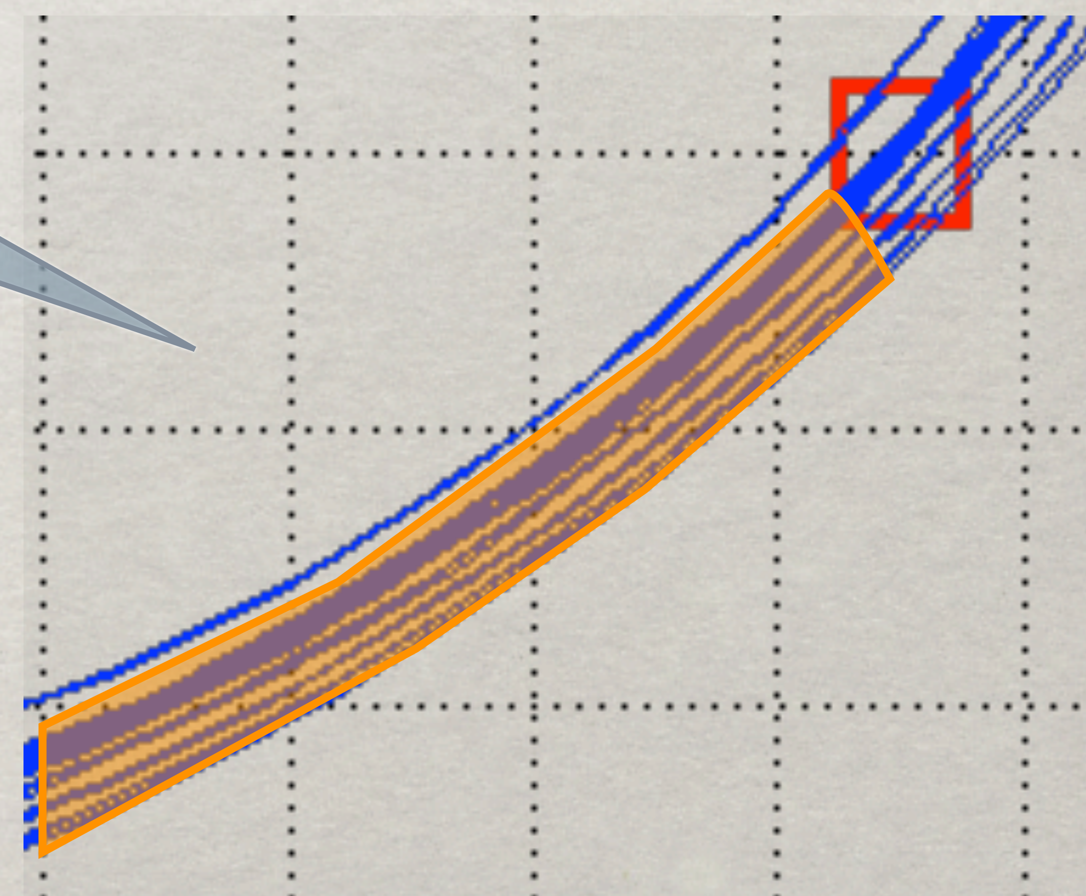

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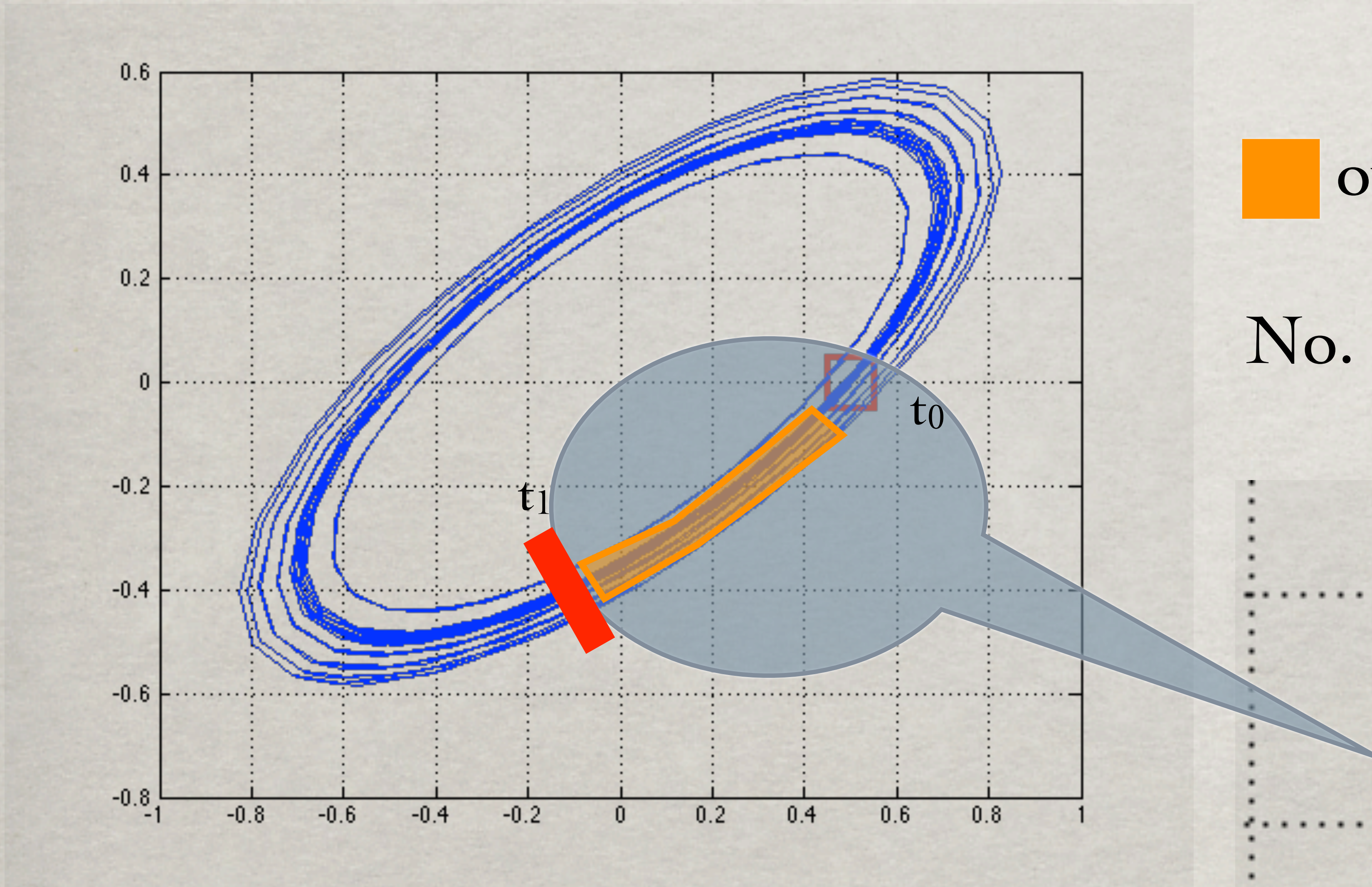

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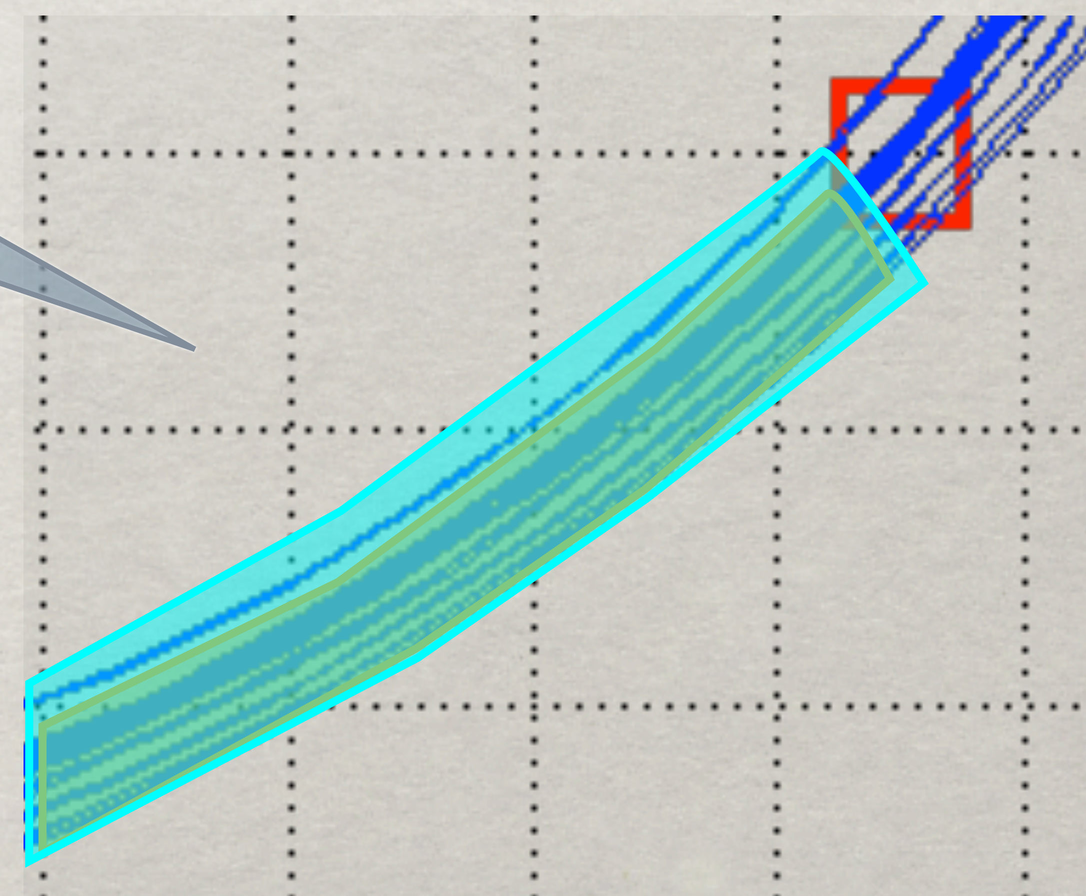
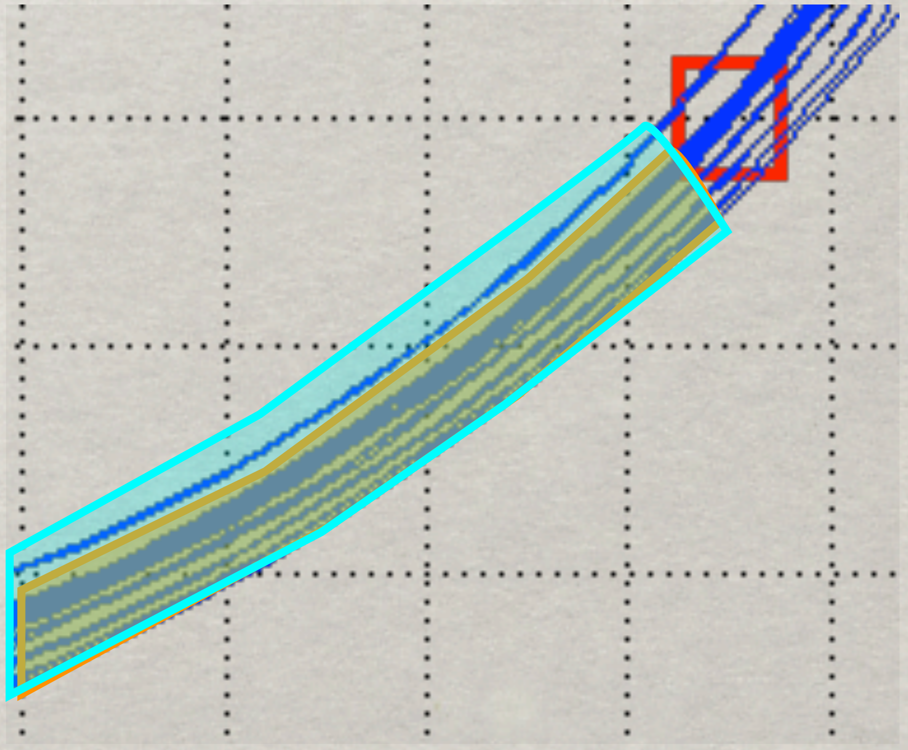


Bloating Flowpipes



Bloating Flowpipes

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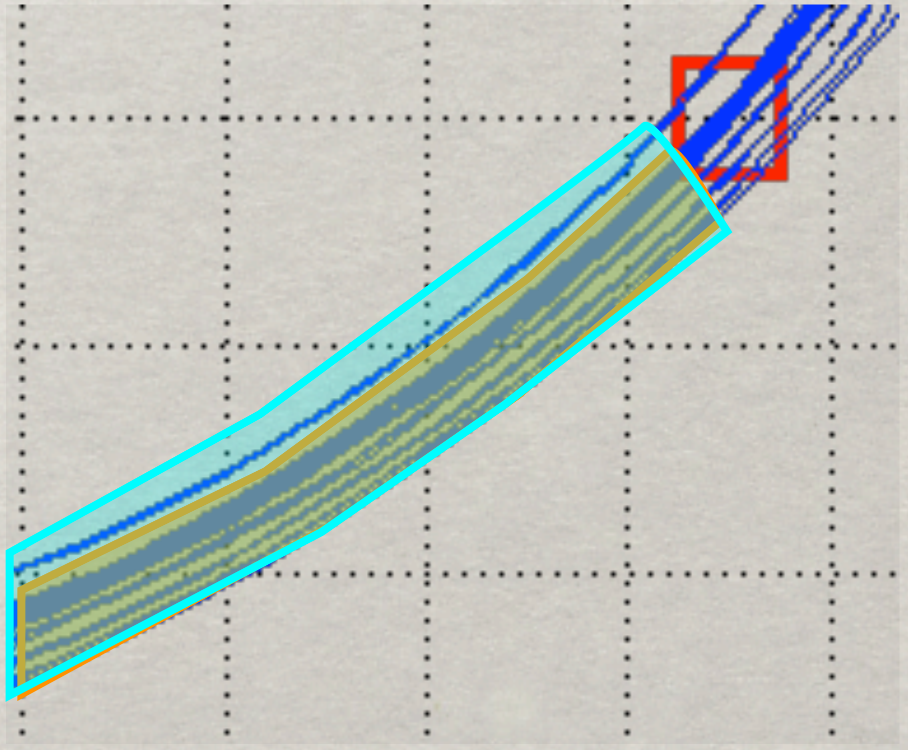

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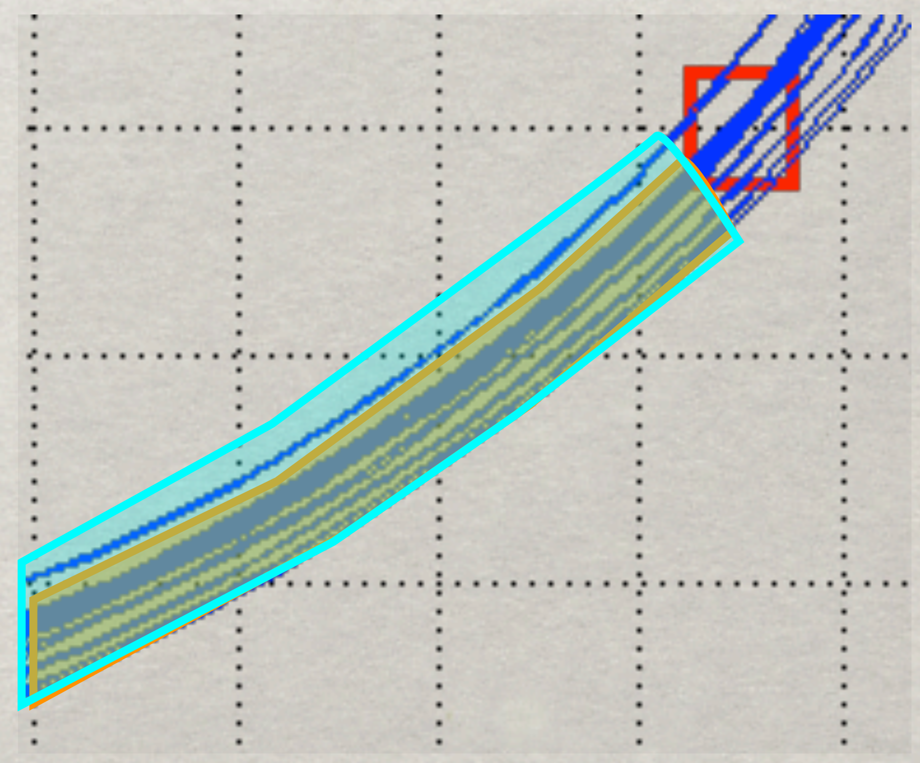

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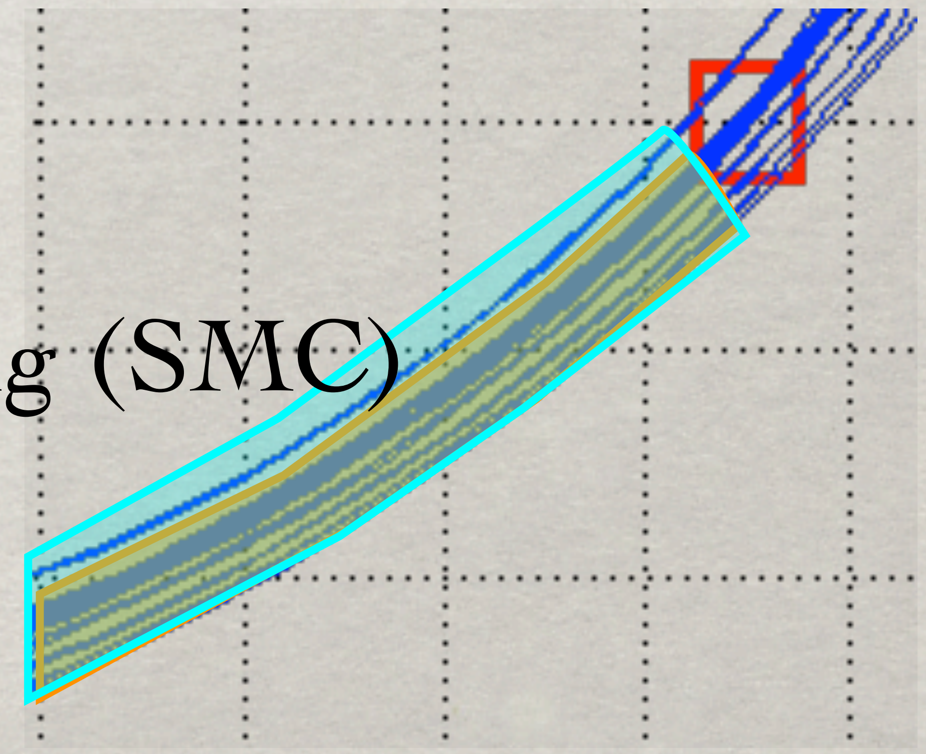
- Ask whether $\vDash P_{(\geq 0.99)}(\varphi)$
  - A statistical model checking (SMC) problem



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- Hypothesis test: H_0: $p \geq 0.99$ vs H_1: $p < 0.99$
  - Sequential probability ratio test (Younes et. al)
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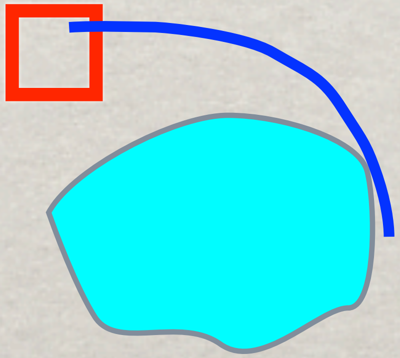

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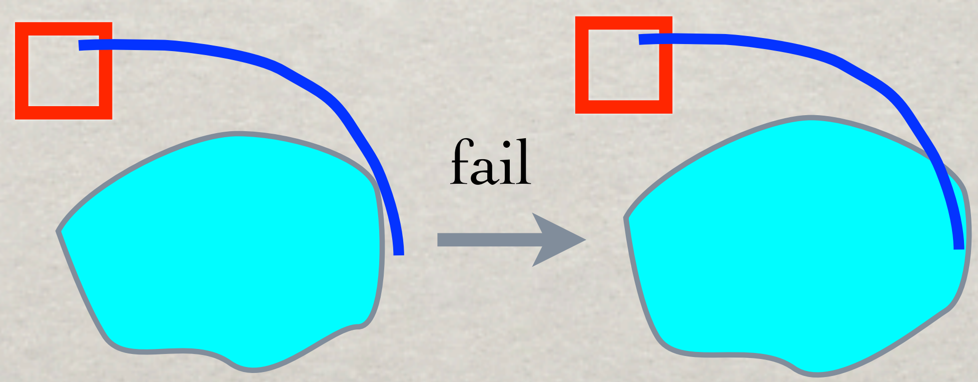

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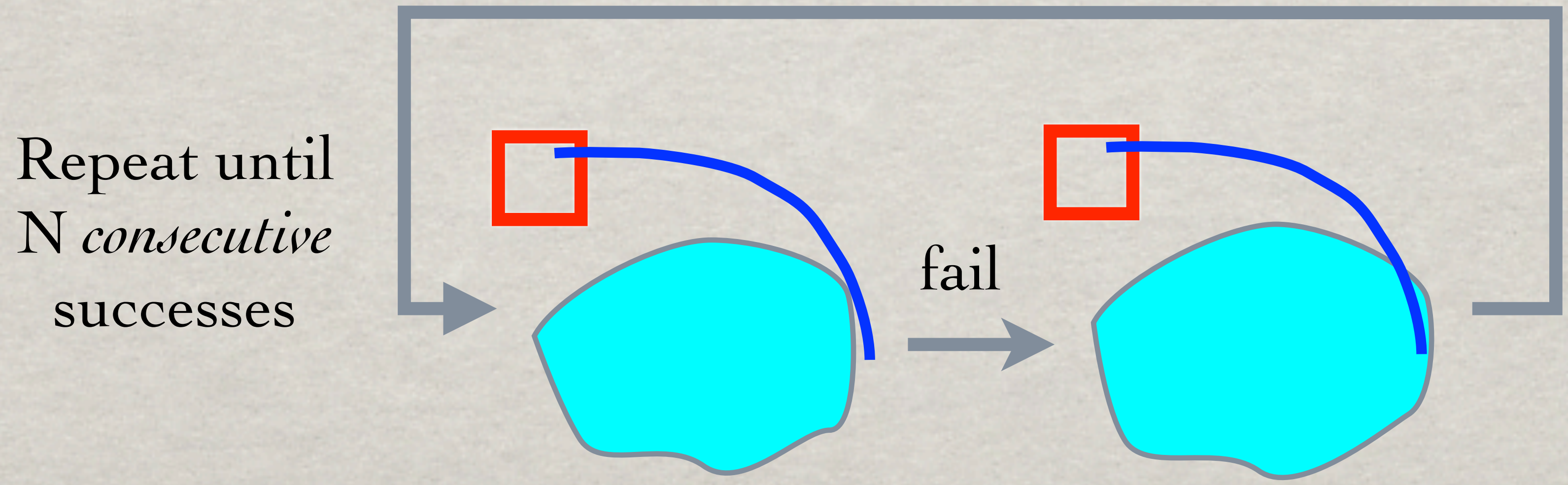

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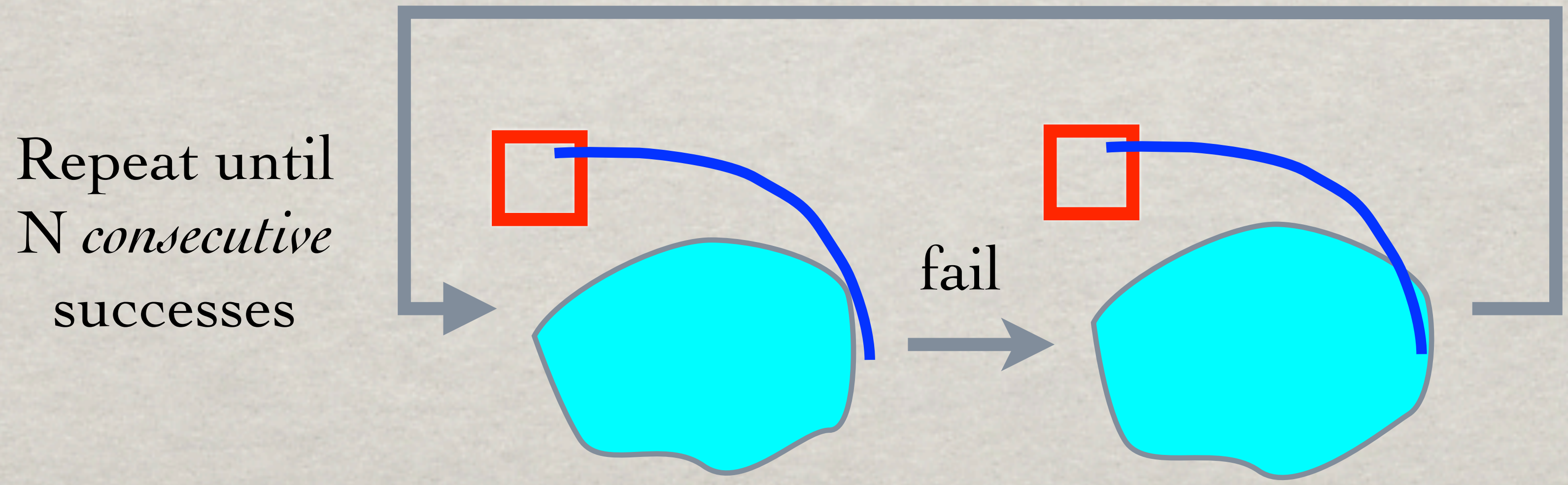
  - Sequential Bayesian test (Clarke et. al)
- Outcome: accept/reject H_0 with specified confidence (usually high, e.g., 0.99)



Empirical Flowpipe Construction

- Sample and simulate
- Compute models to approximate dynamics
- Bloat models for over-approximation

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  ☐ Taylor models (p, I) (Berz et. al)

- Bloat models for over-approximation

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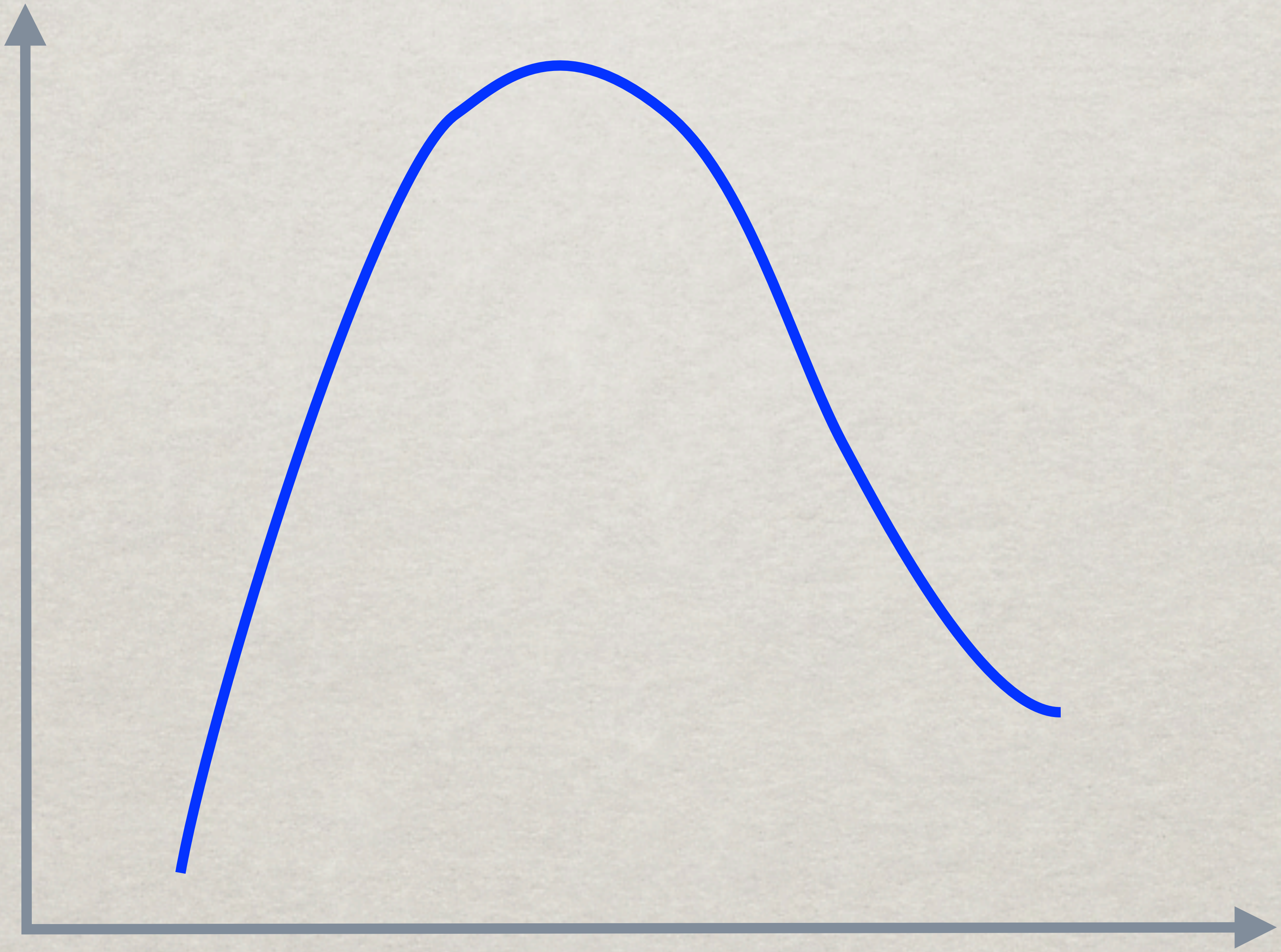
Taylor Models as Flowpipes



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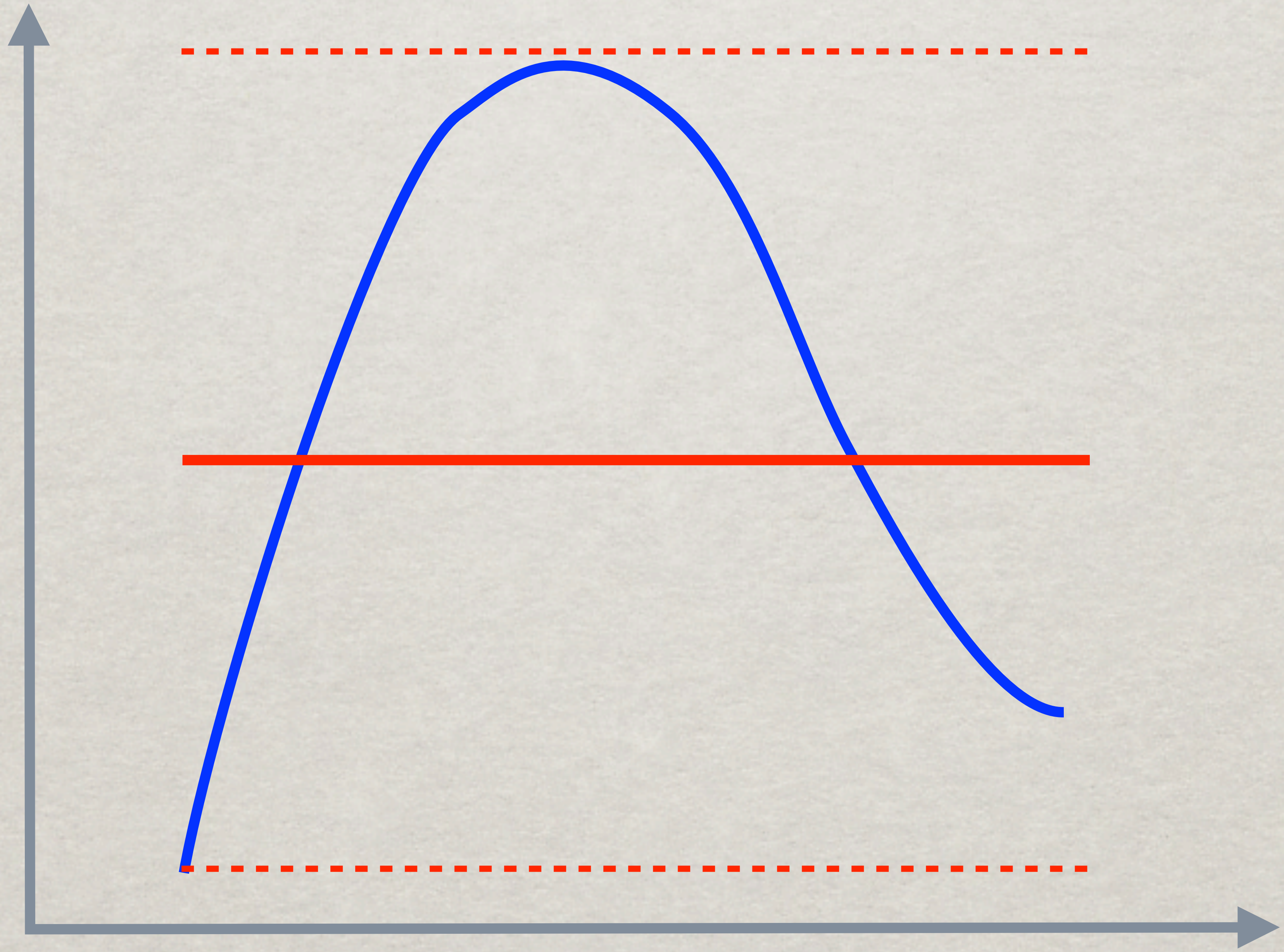

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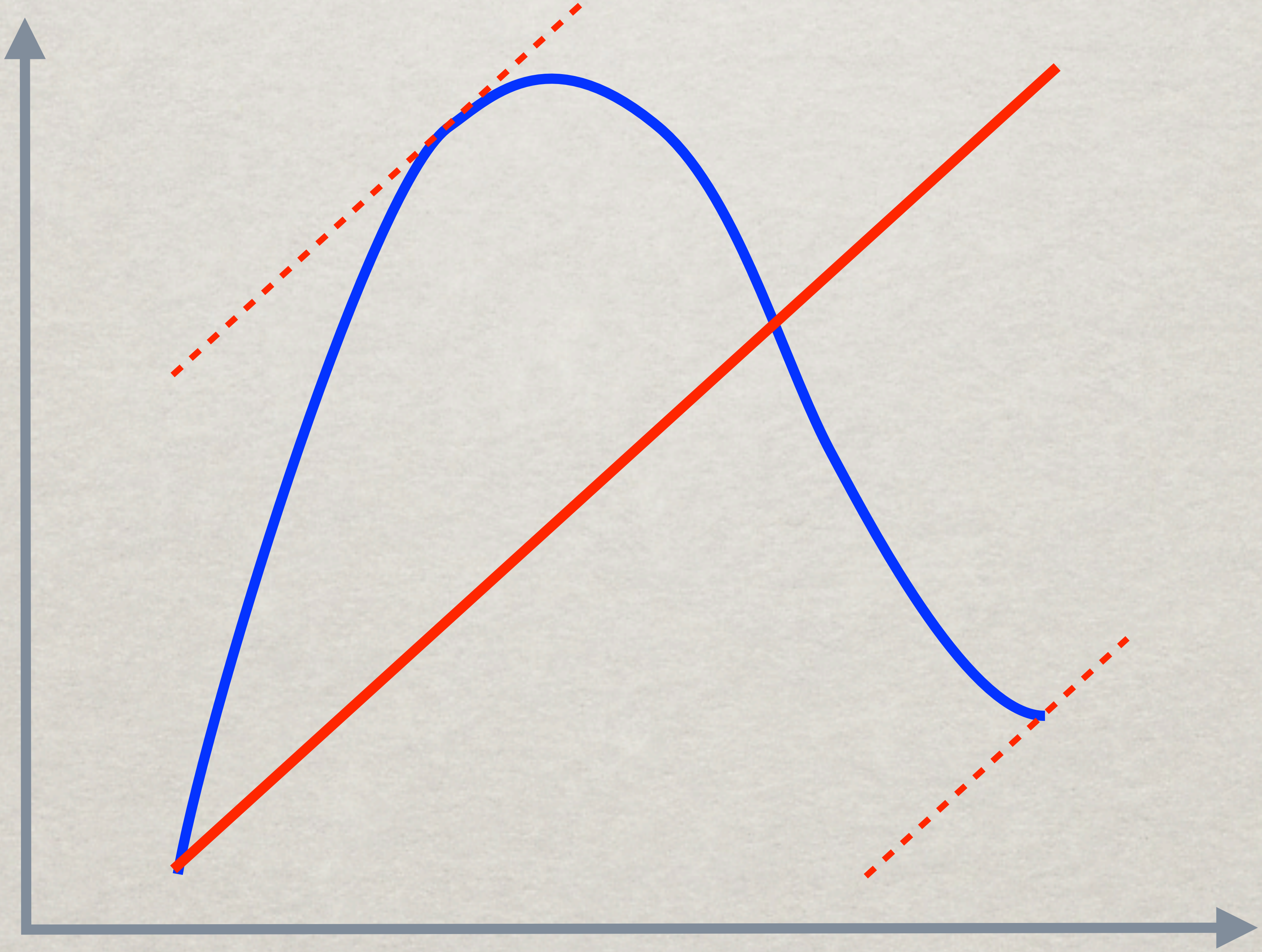

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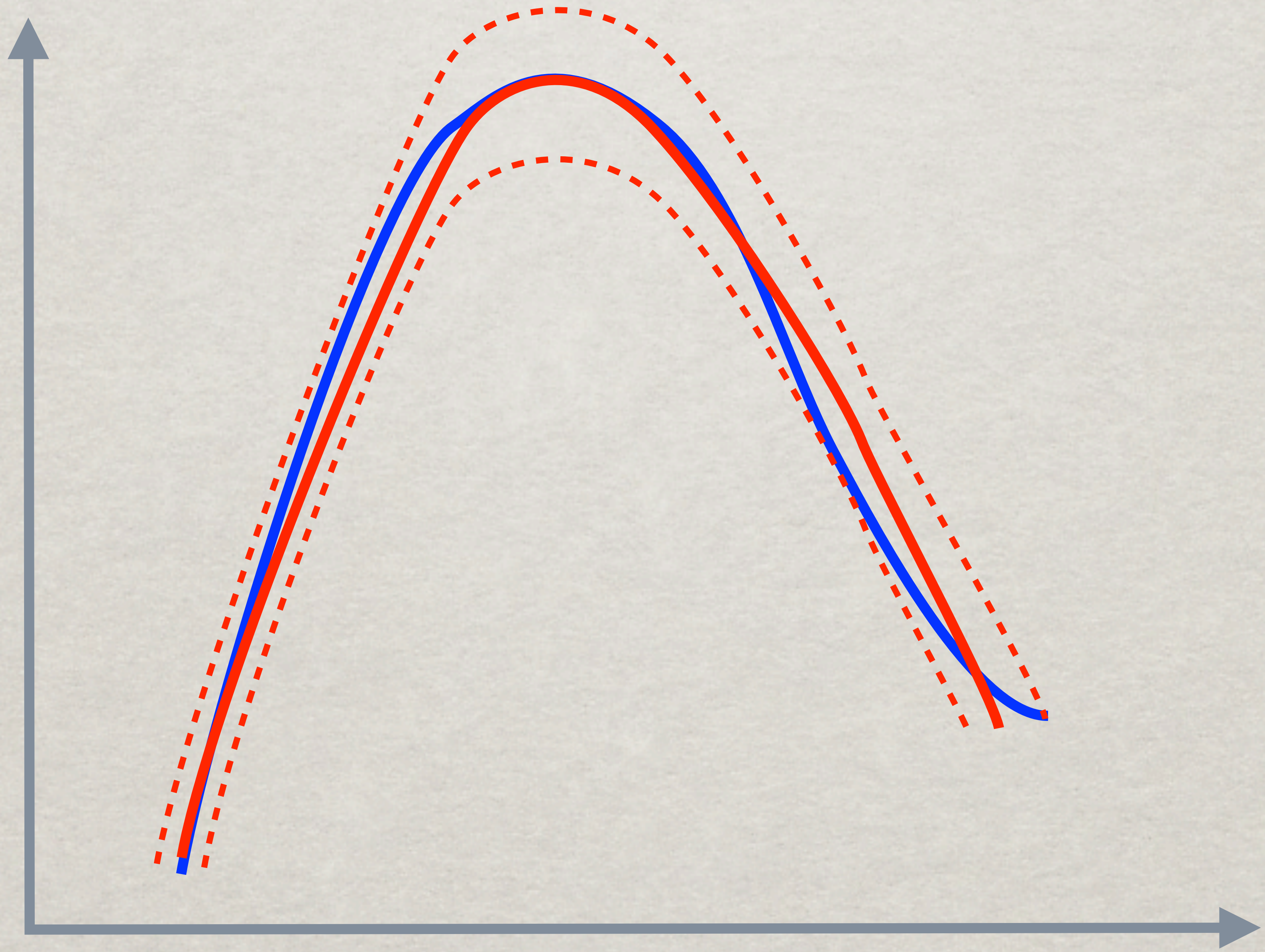
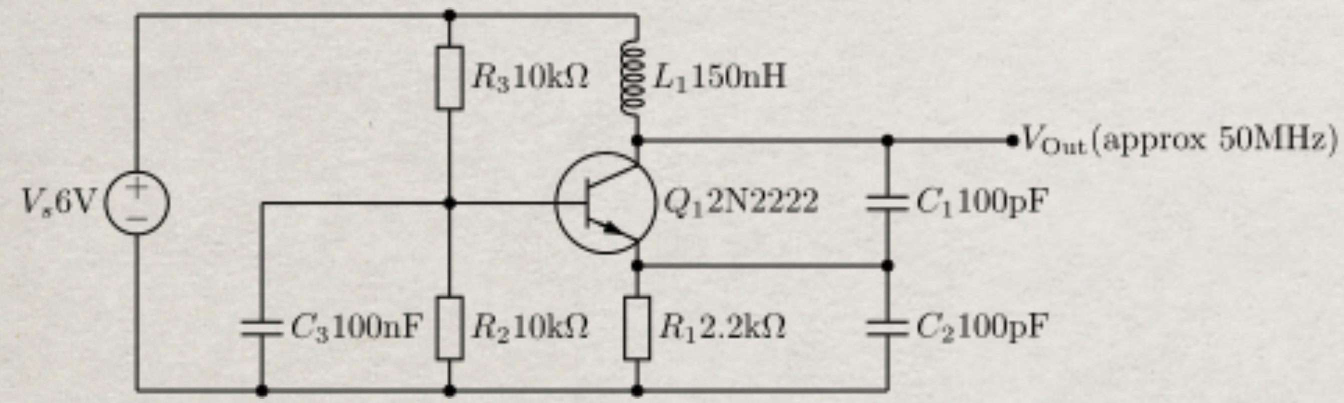


Experiment Results



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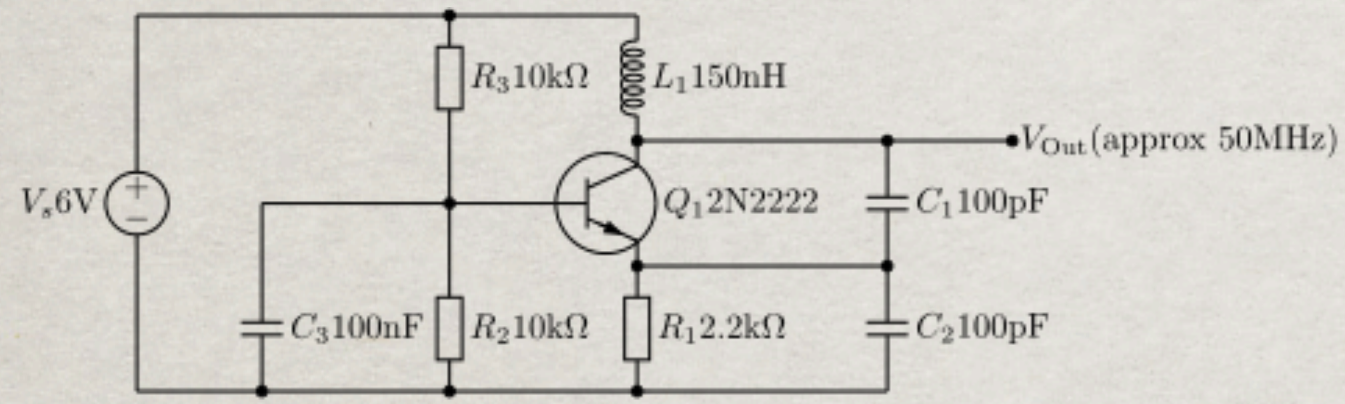

C_1 = 100pF±10%

t∈[0,18ns], 2ns/snapshot

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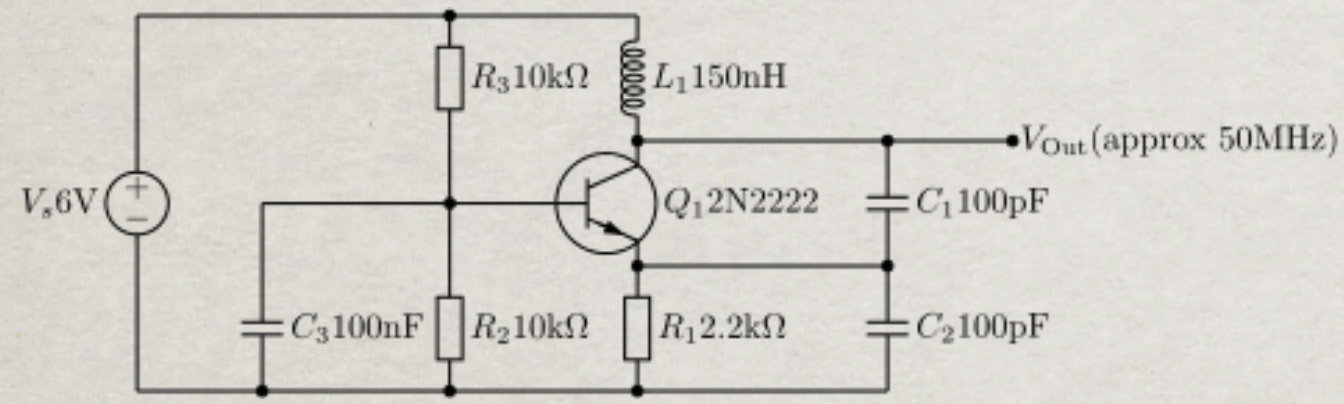

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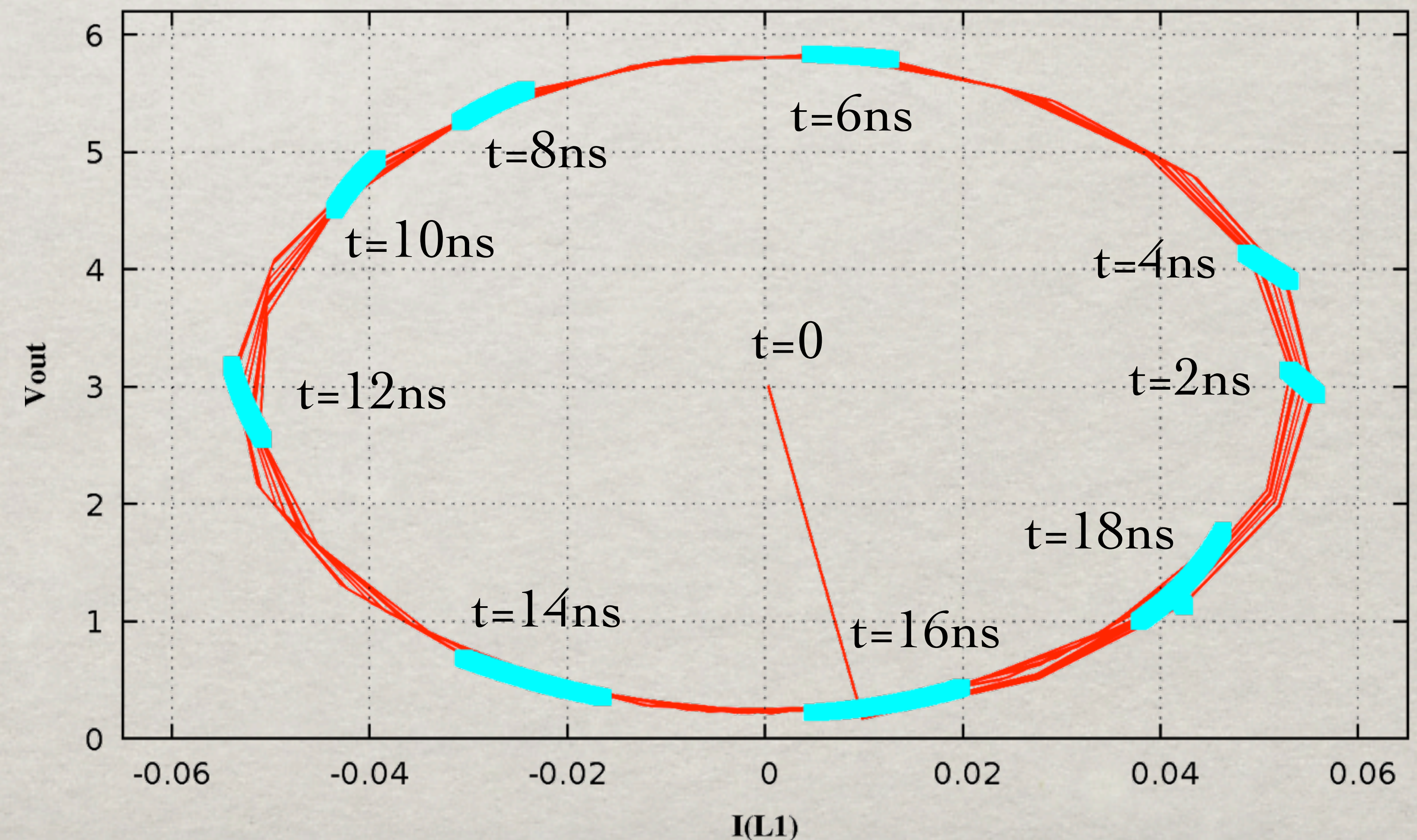

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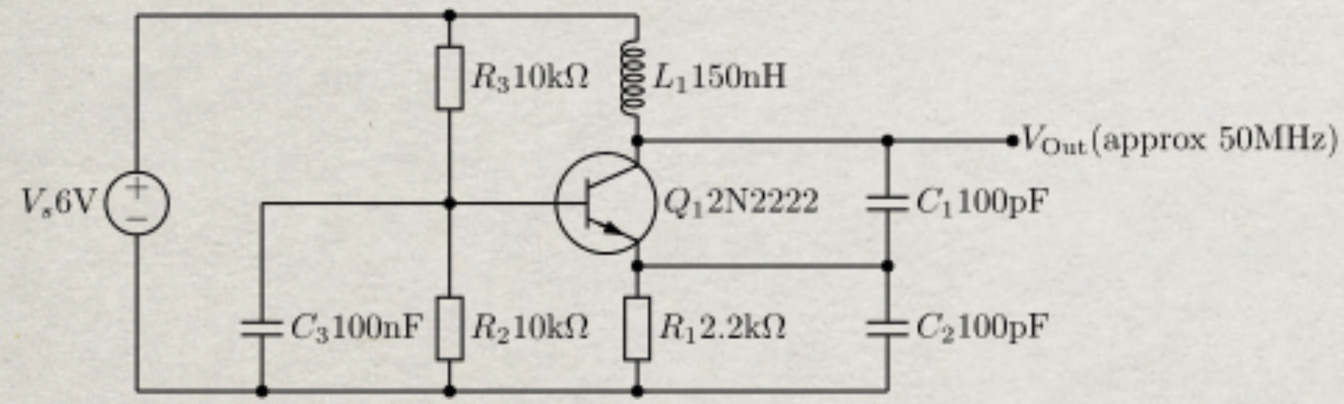

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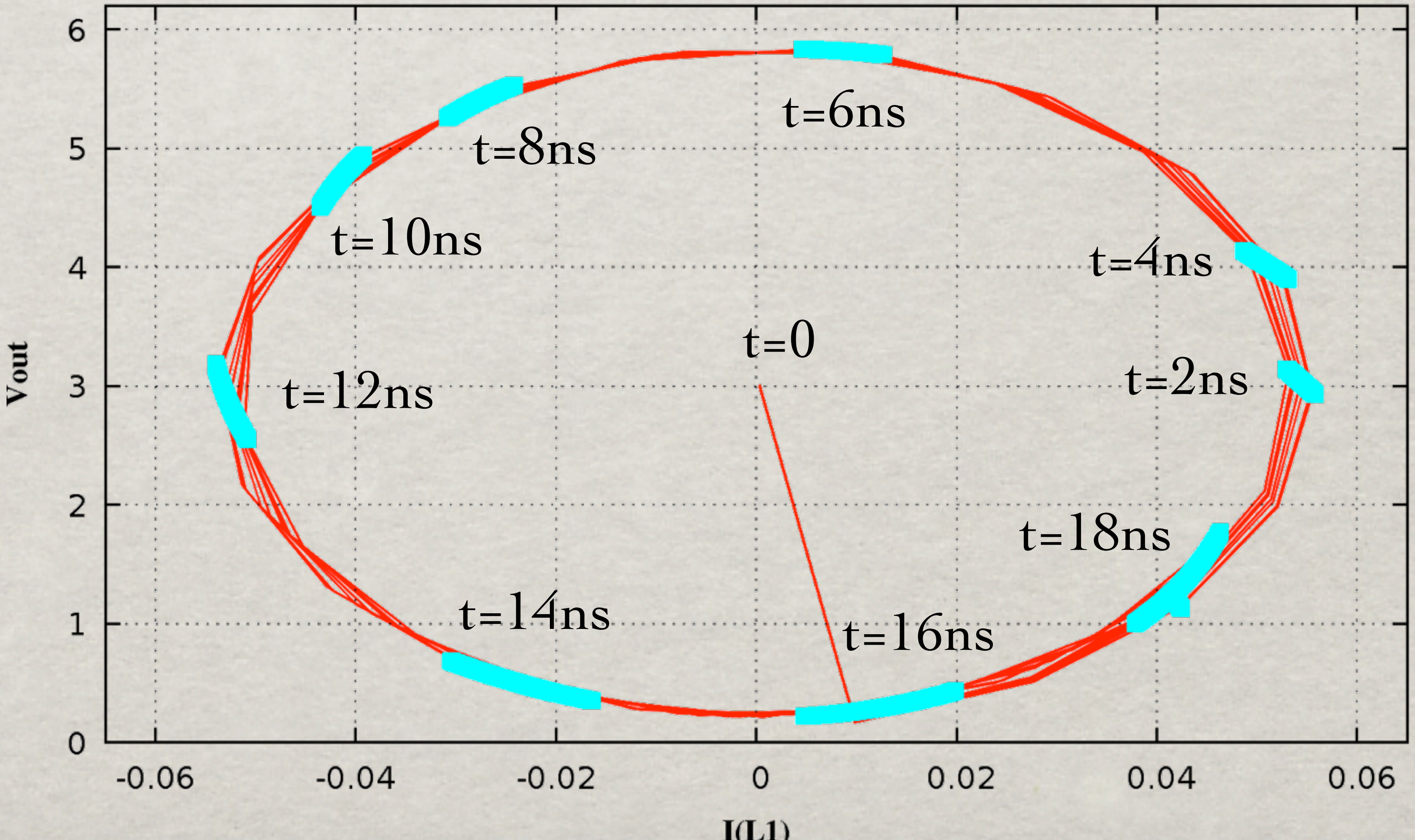
Observations:

- Oscillation
- No limit cycle yet
- Longer flowpipes



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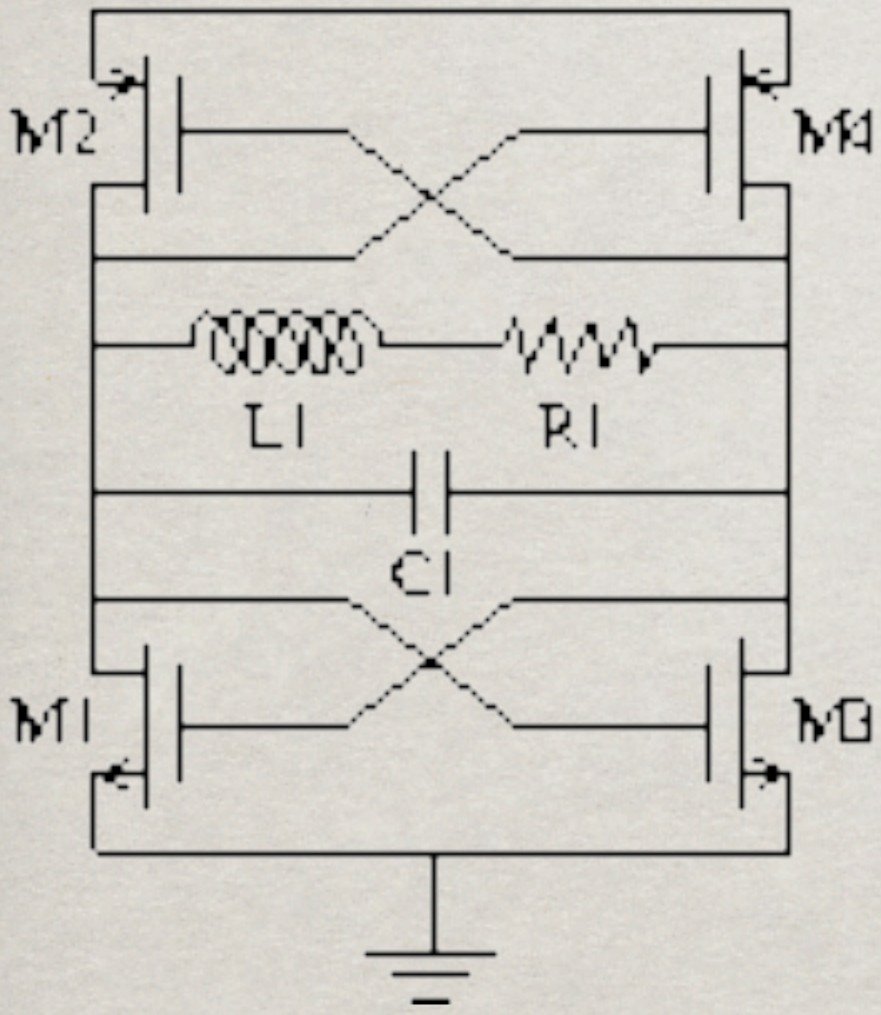

L_1=19.462nH±5%

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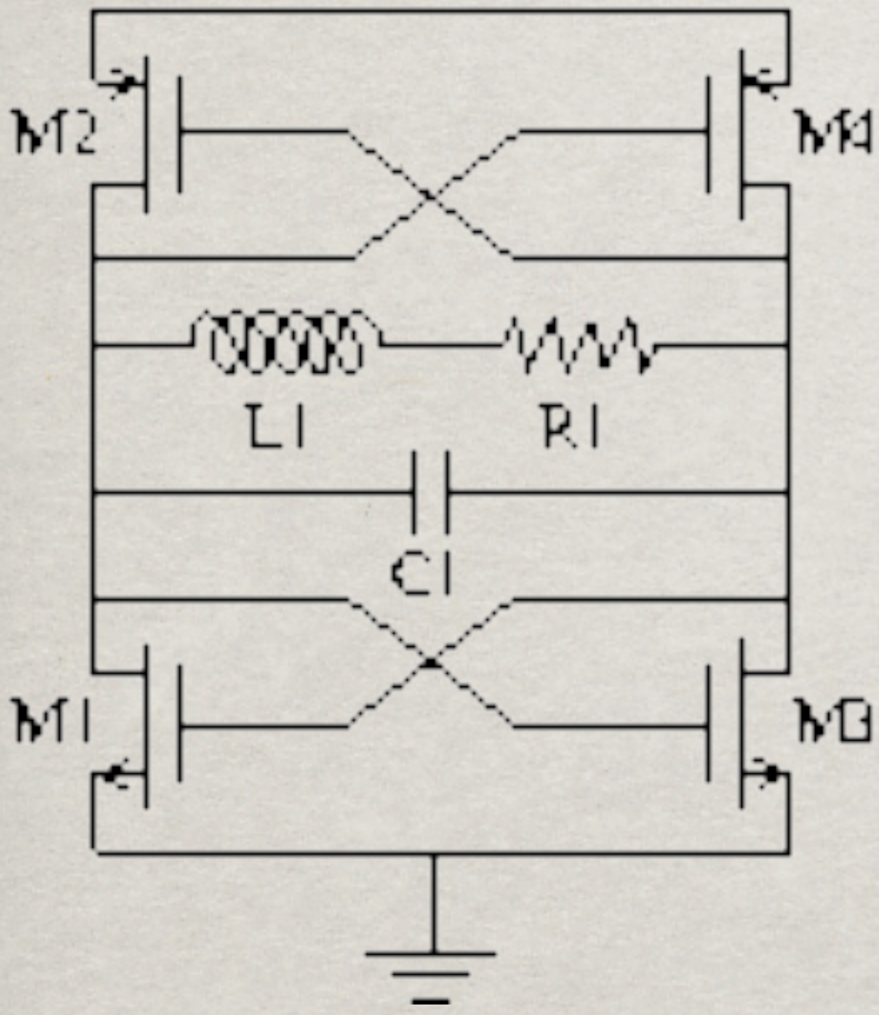

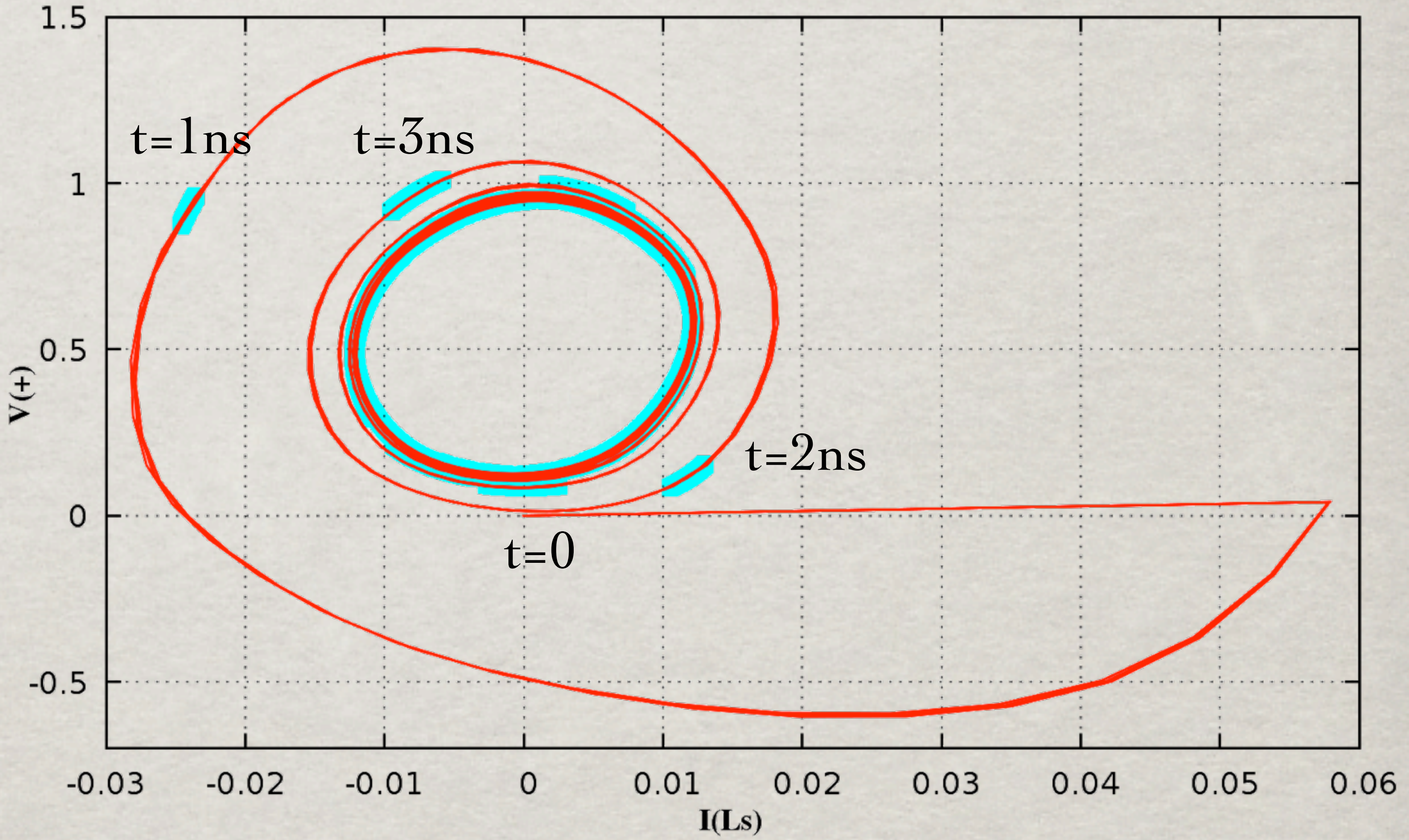

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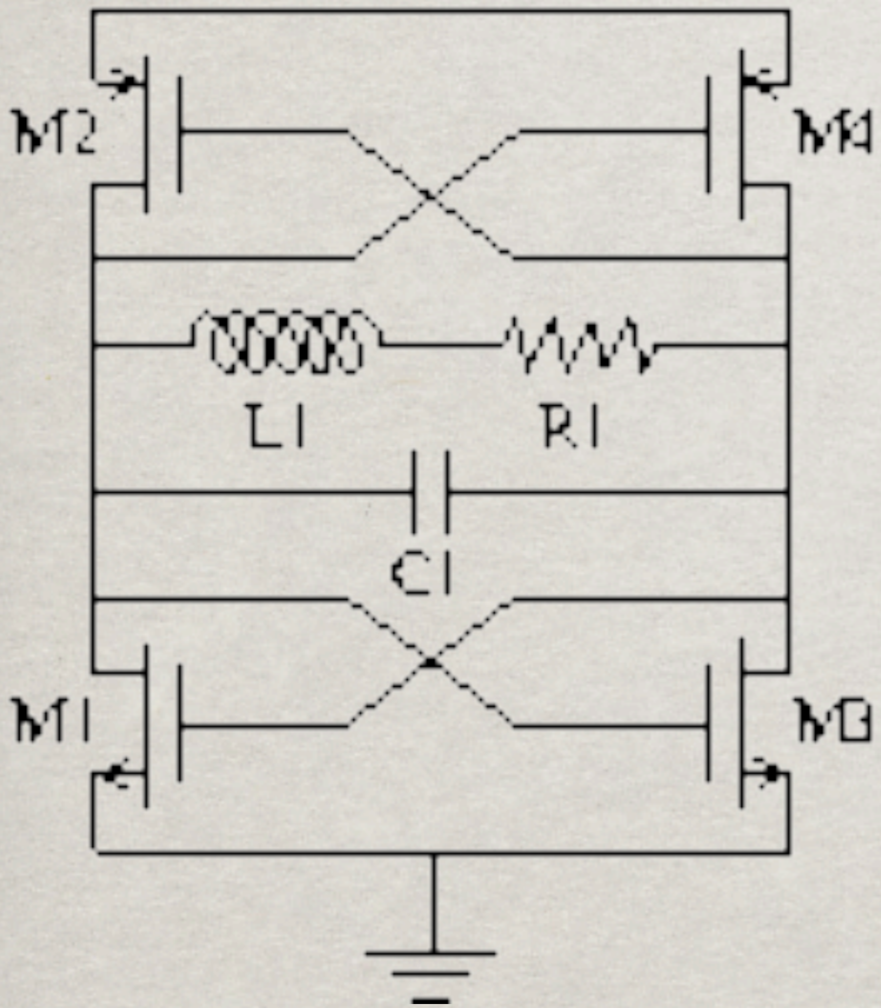

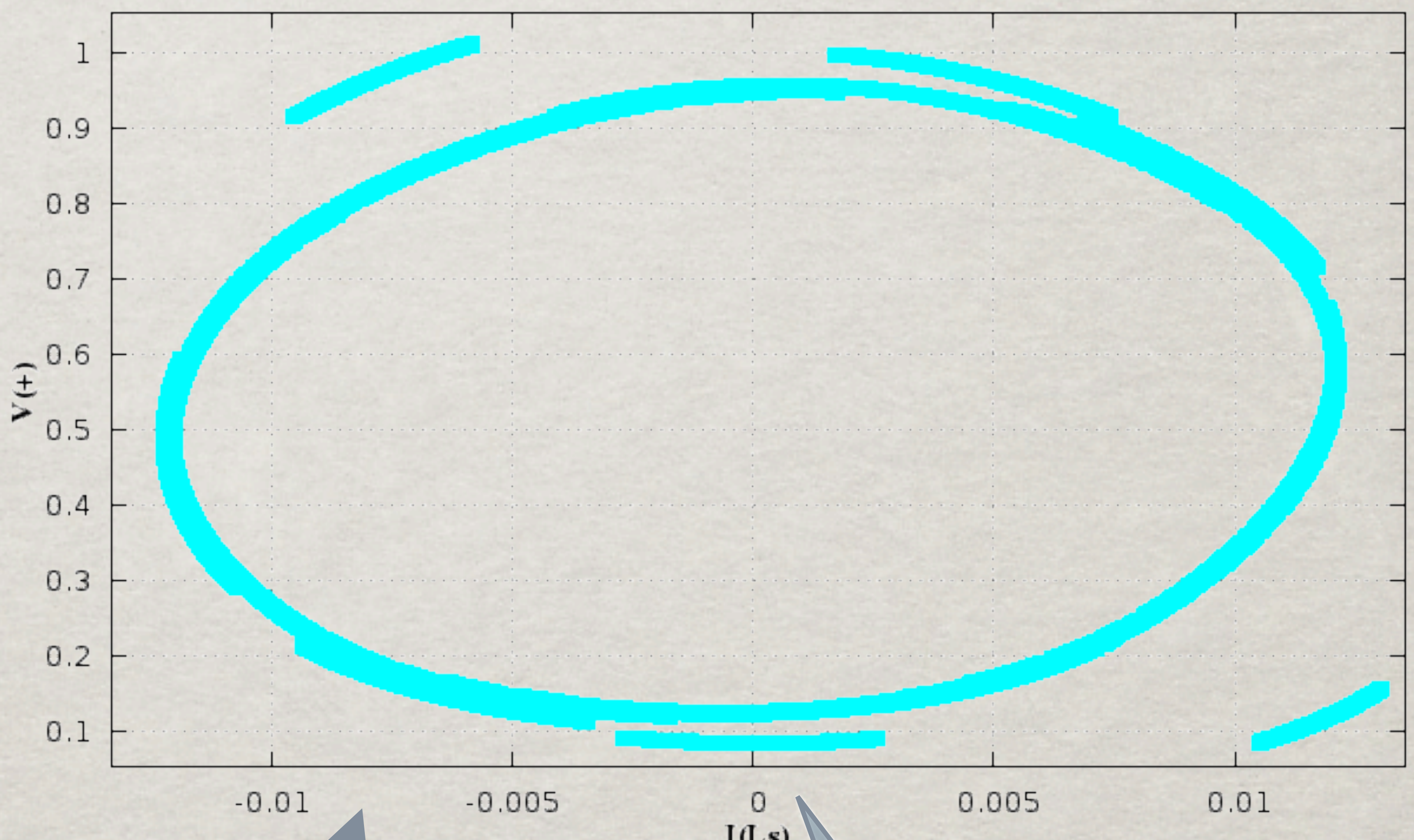

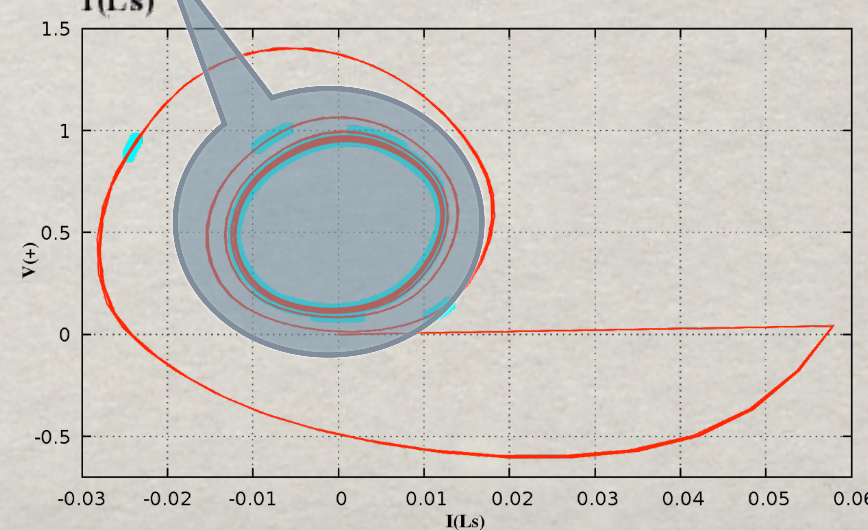

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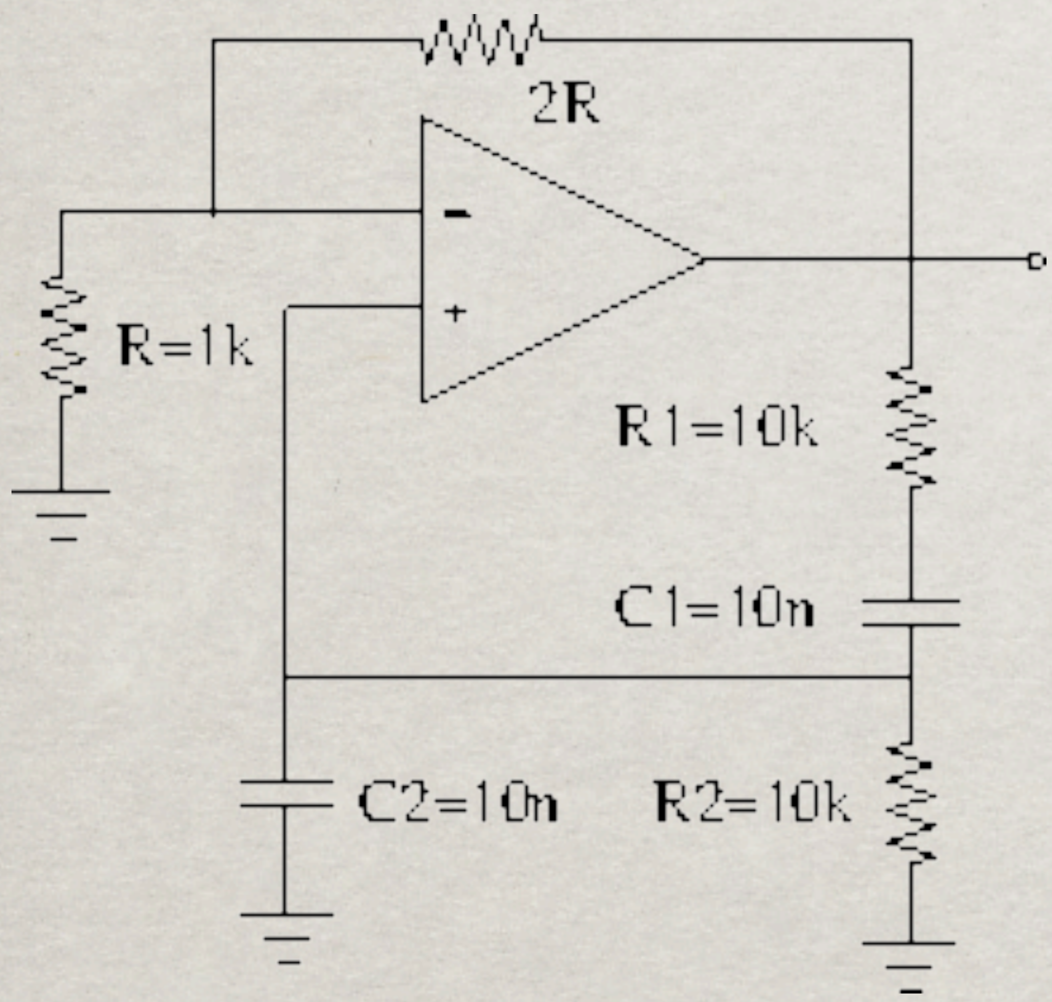

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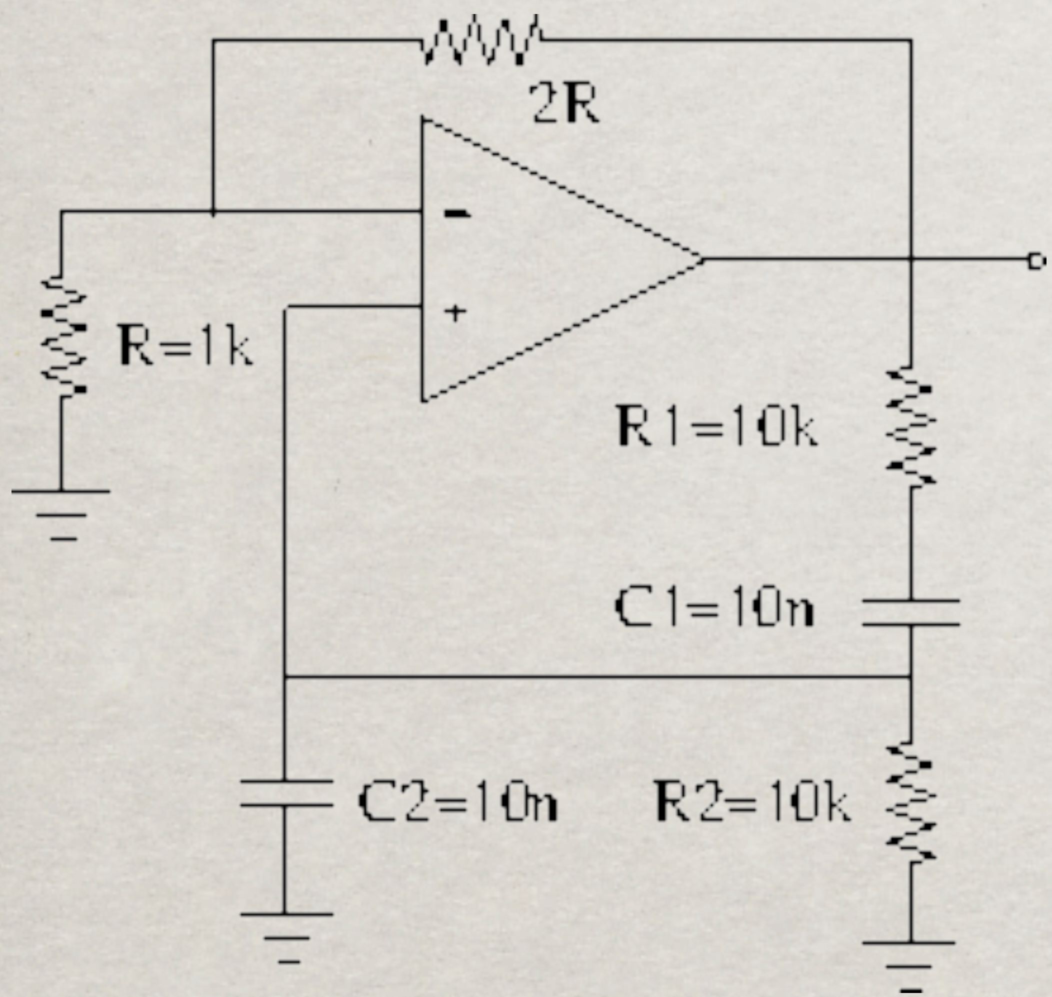

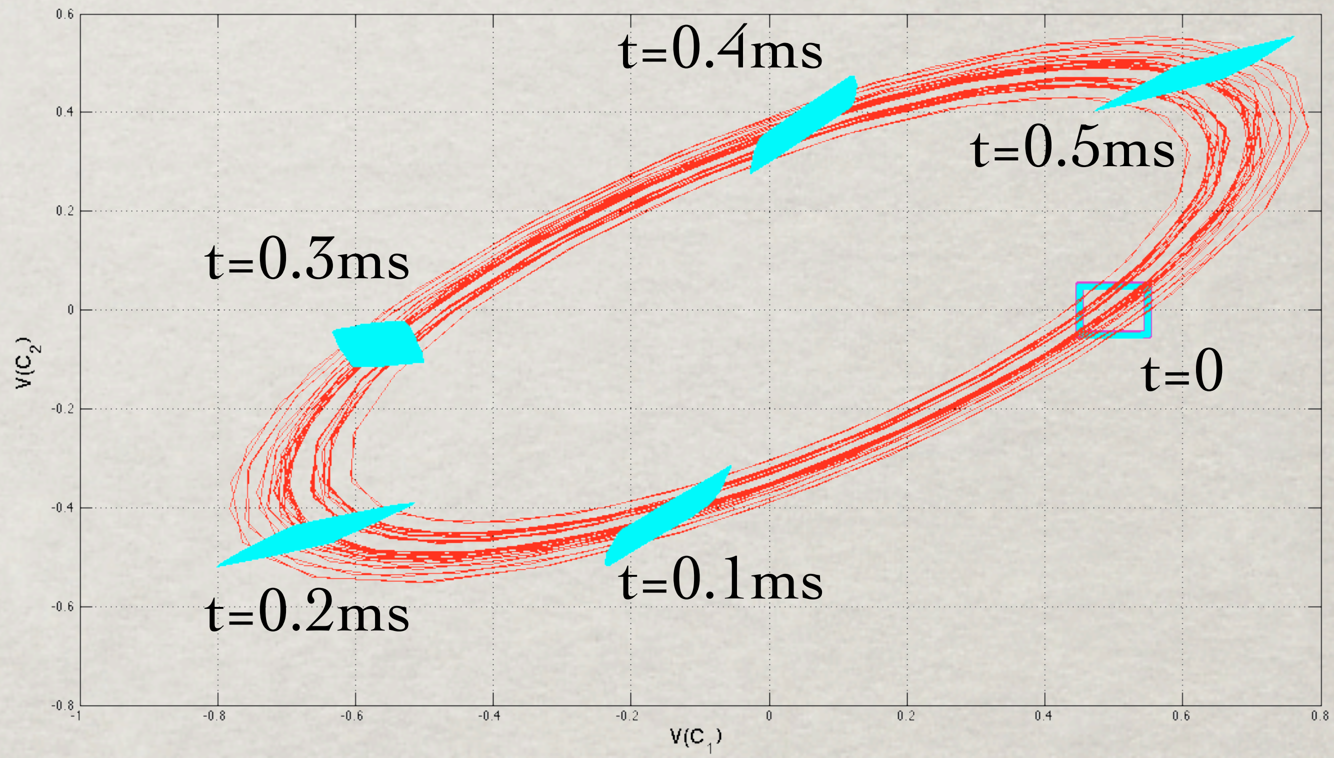

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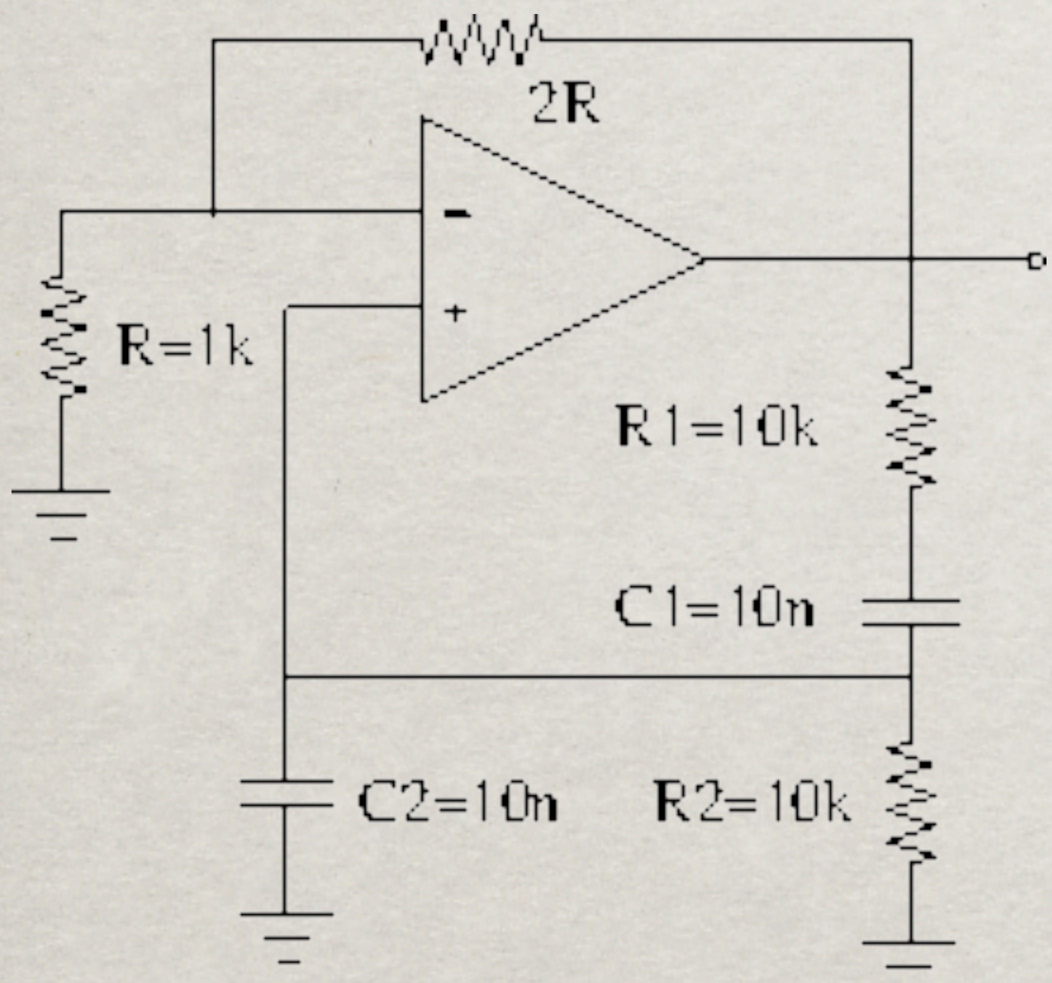

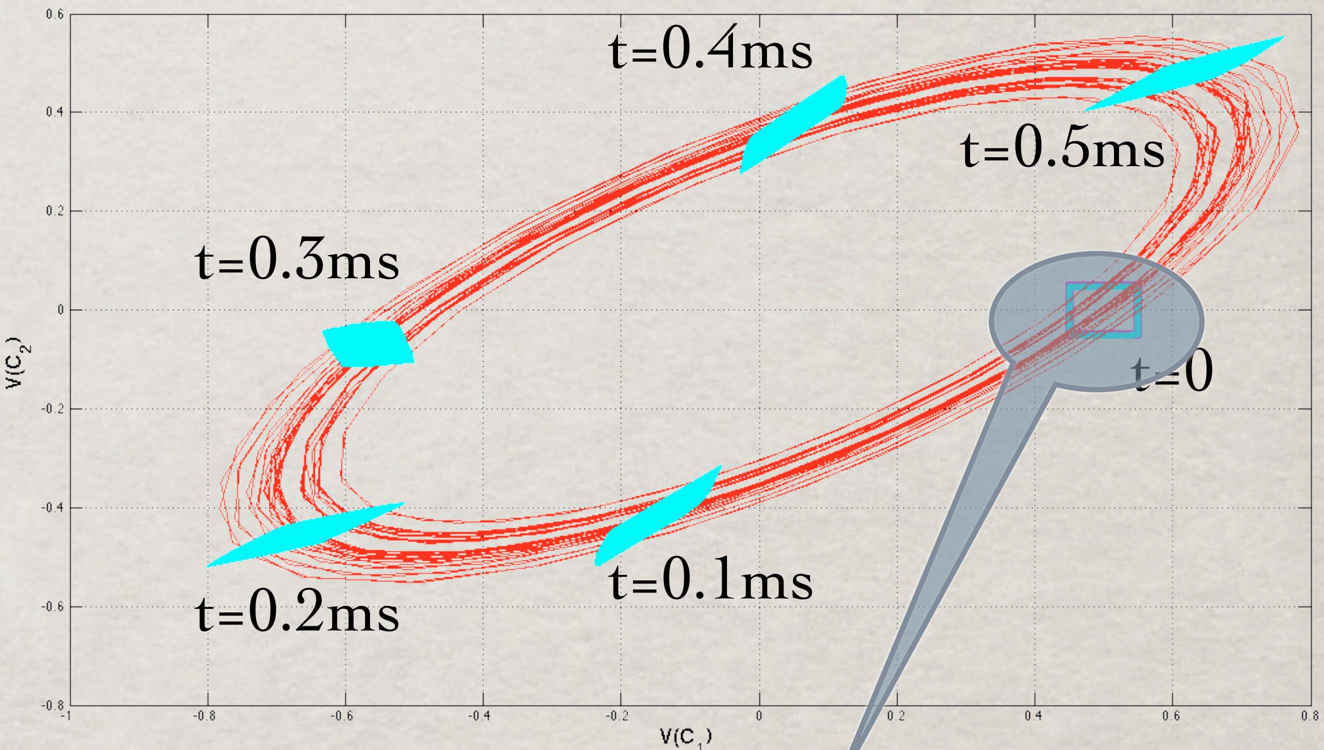

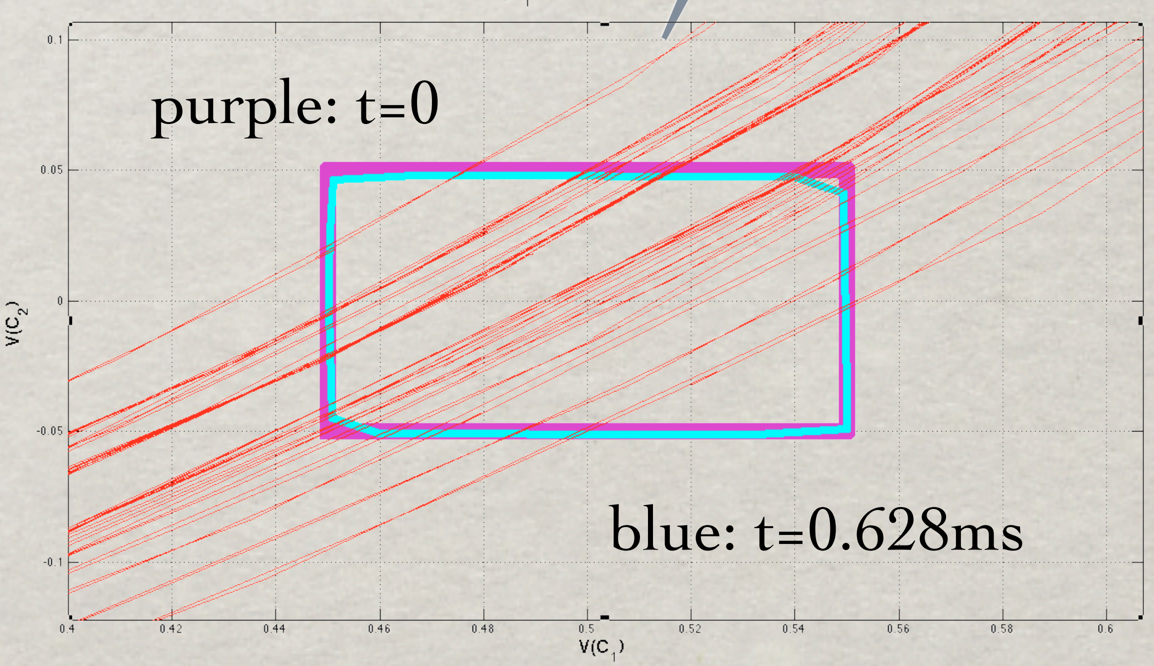

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Conclusion

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- Enable robustness checking
- Enable verification of large circuits

Q & A